Spin-Based Interconnect Technology and Design

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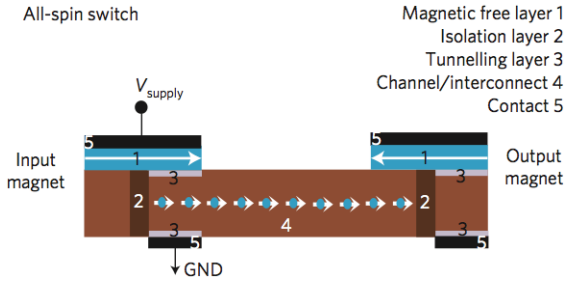
and Ian Young

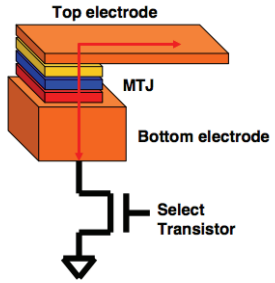
Electron Spin as a Novel State Variable

Electron spin is one of the most widely investigated new state variables to overcome power limit or bring in new functionality.

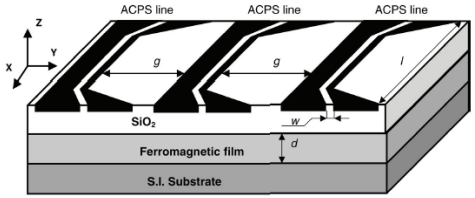
All Spin Logic Device[1]



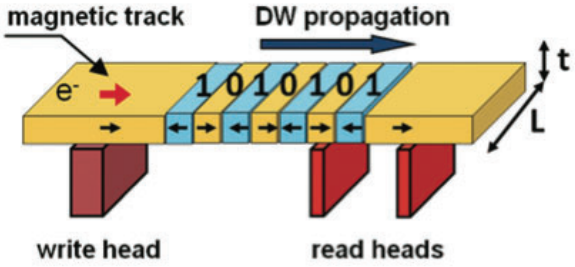
Spin Torque Memory[2]



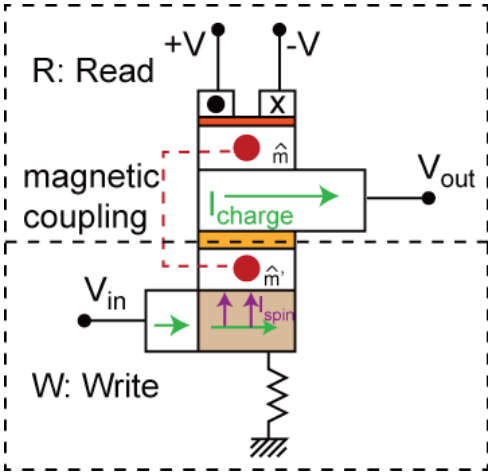
Spin Wave Bus[3]



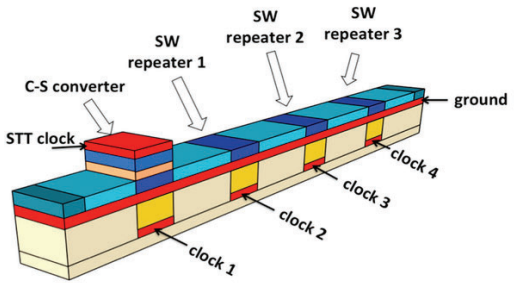
Domain Wall Movement[4]



Giant Spin Hall Current Controlled Logic [5]



Novel Spin Wave Circuit Concept



[1] B. Behin-Aein et al, Nature Nanotechnology, Feb. 2010.
[2] A. Khitun et al, IEEE Tran. Electron Devices, vol. 54, 2007.
[3] X. Wang, Seagate Technology.
[4] W.S. Zhao et al, Jour. App. Phys., 109, 2011.
[5] S. Datta, et al., Applied Physics Letters, 2012.

Why Spintronics in IITC?

Any logic technology must be complemented by compatible interconnects.

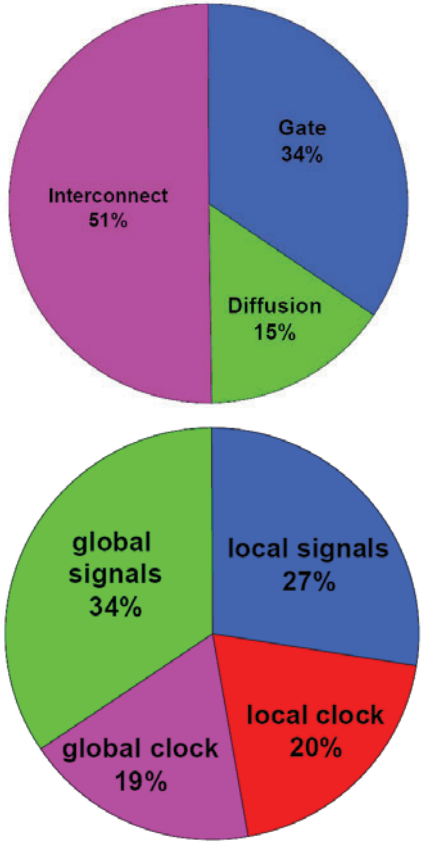
Spintronic components are mostly metallic.

Spintronics can be embedded in BEOL to augment CMOS

The boundaries between interconnects and devices are blurred in some beyond CMOS spintronic logic.

Interconnect Challenge

Total Dynamic Power Breakdown @ 0.13µm

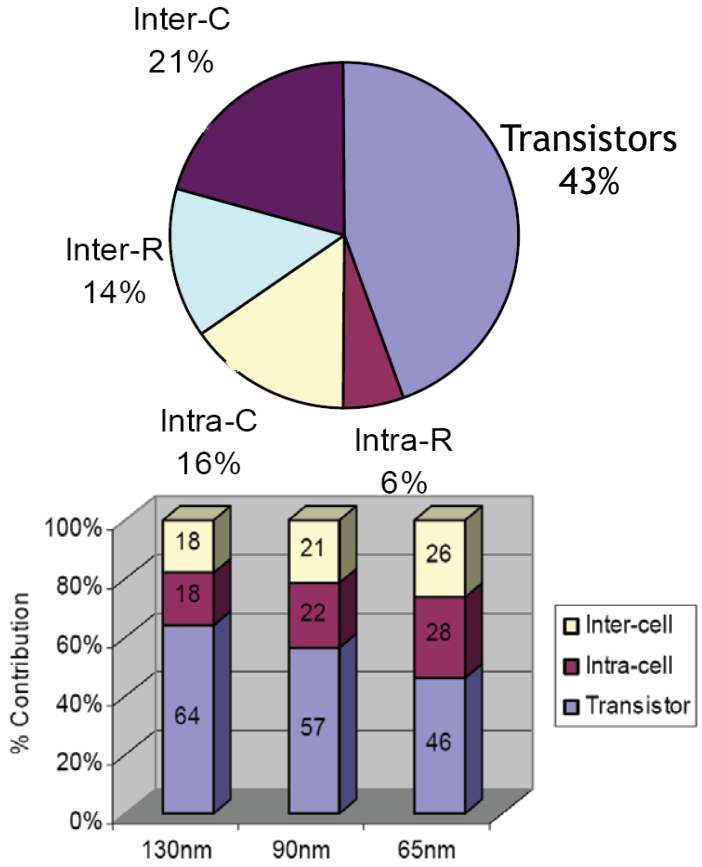


Data from Intel,
N. Magen et al., *SLIP Workshop*, 2004.

Interconnects are an ever growing challenge.

Local and global interconnects are both important in terms of power dissipation and speed.

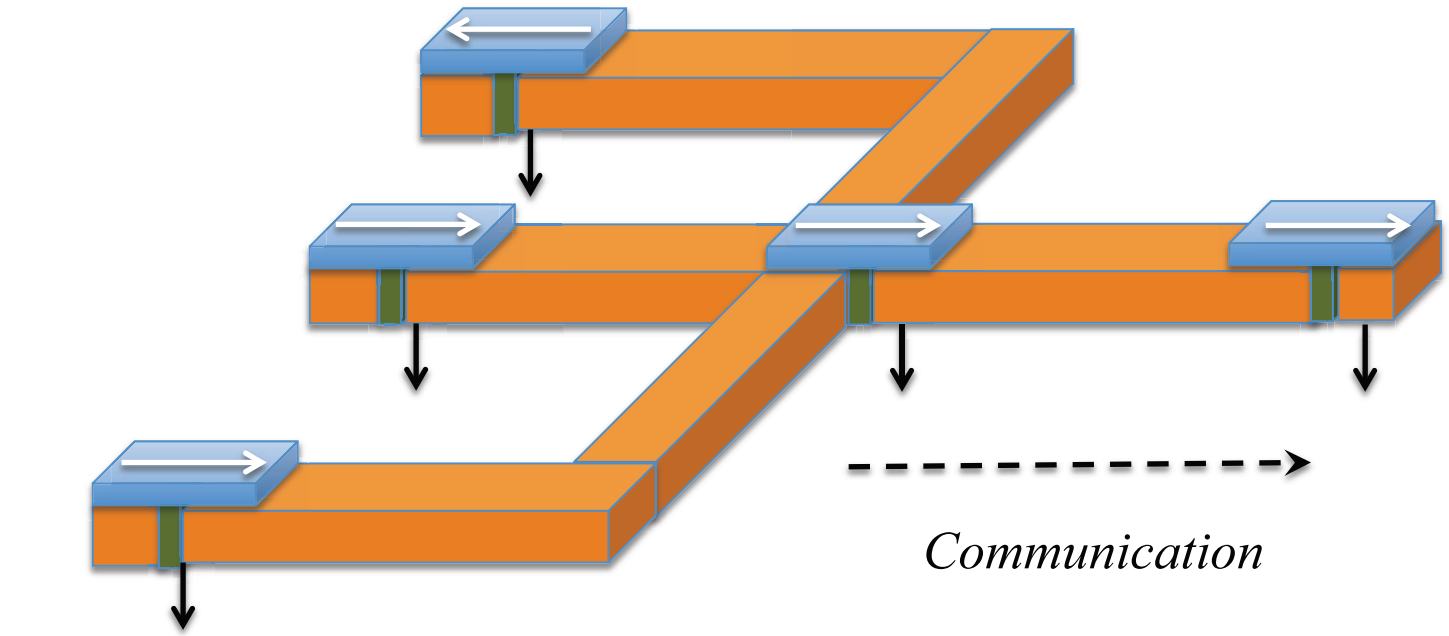
% Composition of Circuit Delay (NAND2 FOM short routes)



Nagaraj NJ from Texas Instruments, SRC Interconnect Forum, Sept. 2006.

Computation and Communication

The boundary between devices and interconnects is blurring.



B. Behin-Aein, et al., ”Proposal for an all-spin logic device with built-in memory,” Nat. Nanotechnol., vol. 5, no. 4, pp. 266-270, 2010.

Hierarchy of Limits: Si Microelectronics

	Major Options	Example Key metrics
System	RISC, CISC, …	Throughput (IPS), power density, …
Circuit	Static CMOS, dynamic, …	Noise margin, delay, variability,
Device	MOSFET Metallic wires	Delay, Energy per binary switching operation, standby power
Material	Si Al, Cu SiO2	Mobility, saturation velocity Resistivity Break down field
Fundamental	Speed of light, Laws of thermodynamic Atom size	Time of flight, Thermal noise

J. D. Meindl, *Science*, 2001.
J.D. Meindl, *Proc. IEEE*, 1995.

Hierarchy of Limits: Beyond-CMOS Nanoelectronics

	Major Options	Example Key metrics
System	RISC, CISC, Nontraditional	Throughput (IPS), power density, …
Circuit	Static CMOS, dynamic, majority gates, Neuromorphic Computing…??	Error rate, delay, variability, power
Device	Thermionic FETs Tunnel FETs Magnetic/spintronic Nanomechanical switches …??	Delay, Energy per binary switching operation, standby power
Material	Si, GaAs, Al, Cu, Carbon Nanotubes, Graphene, Other 2D materials, Ferromagnets, …???	Mobility, saturation velocity Resistivity, spin relaxation time,
Fundamental	Speed of light, Laws of thermodynamic Atom size	Time of flight, Thermal noise Spin magnetic moment of electron

State Variables

For Logic Devices:

Nonreciprocity

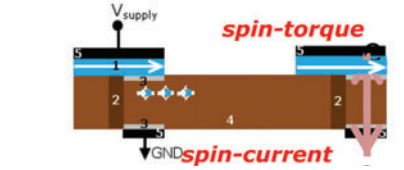
Gain

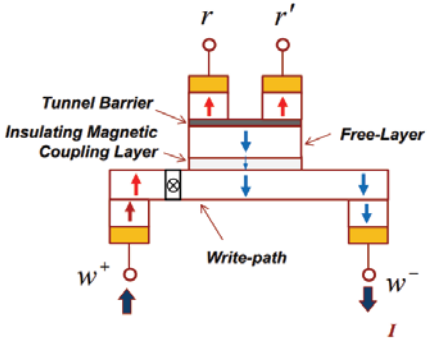
Read/Write compatibility

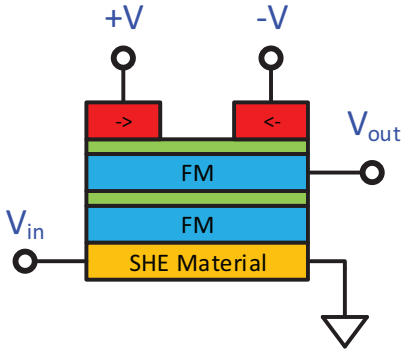
Write	State Variable	Read

ASL	Spin Transfer Torque	Magnetic Dipole	Spin Filtering
mlogic	Spin Transfer Torque	Magnetic Dipole (Domain Wall)	Tunnel Magnetoresistance
CSL	Spin Hall Effect + Dipolar Coupling	Magnetic Dipole	Tunnel magnetoresistance

Current Controlled







[1] B. Behin-Aein et al, Nature Nanotechnology, Feb. 2010.

[2] Currivan, Jean Anne, et al.“" *Magnetics Letters*, (2012)

[3] [5] S. Datta, et al., Applied Physics Letters, 2012.

State Variables

For Logic Devices:

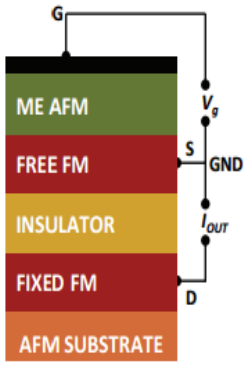
Nonreciprocity

Gain

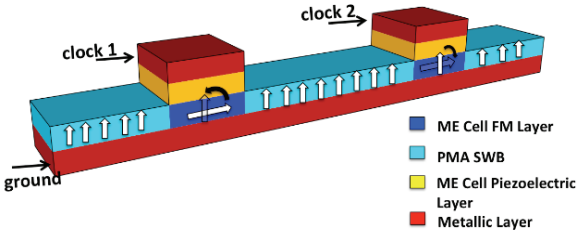
Read/Write compatibility

Write	State Variable	Read

MEMTJ	Exchange Bias	Magnetic Dipole	Tunnel magnetoresistance
SWD	Magnetostriction + spin wave tilting	Magnetic Dipole	Magnetostriction + spin wave tilting



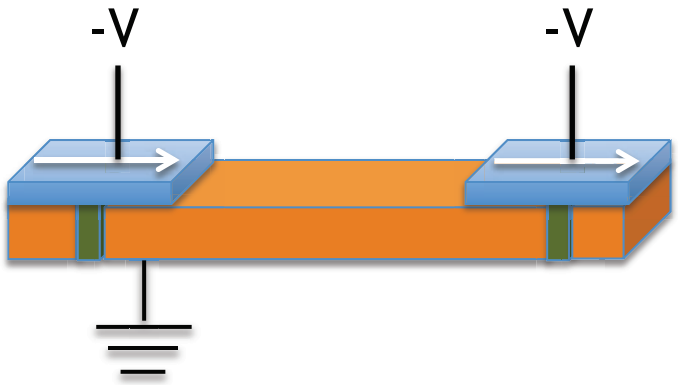
Voltage Controlled



[1] Sharma, Nishtha, et al. , Energy Efficient Electronic Systems (E3S), 2015 Fourth Berkeley Symposium on. IEEE, 2015.

[2] S. Dutta, et al., Nature Scientific Report, 5, Article number: 9861 (2015)

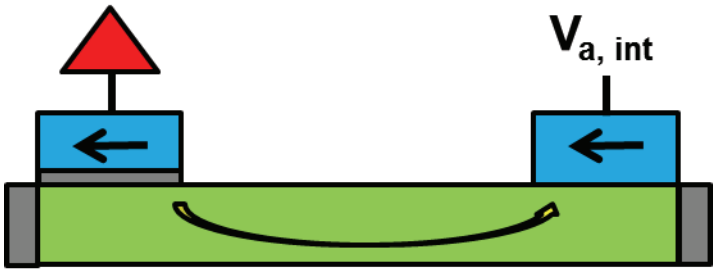
Drift-Diffusion Spin Devices/Interconnects



Non-Local Spin torque configuration provides non-reciprocity.

Channel material: Metals such as Cu, Al

B. Behin-Aein, et al., "Proposal for an all-spin logic device with built-in memory," Nat. Nanotechnol., vol. 5, no. 4, pp. 266-270, 2010.



A tunnel barrier in a conventional spin torque device blocks electrons from moving back to the transmitting magnet.

Channel material: Cu, Al, Si

D. Datta, et al., "Voltage Asymmetry of Spin-Transfer Torques," IEEE Trans. Nanotechnol., vol. 11, no. 2, pp. 261-272, Mar. 2012.

Outline

- Introduction
- Spin Drift/Diffusion Devices and Interconnects
  - Materials
  - Devices
  - Circuits & systems
- Spin Wave Circuits
- Conclusions

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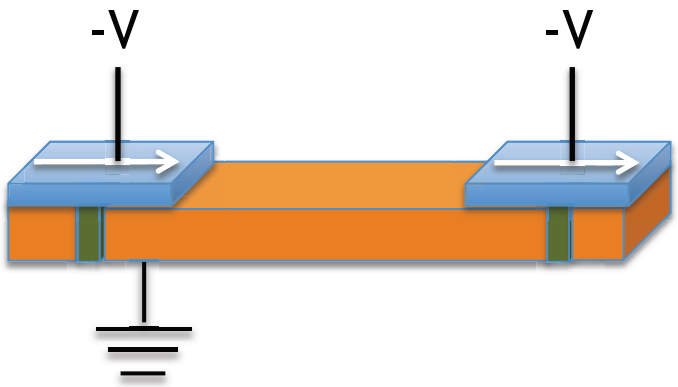
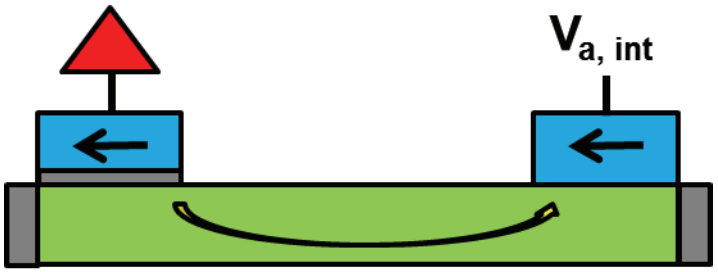
Important Material Properties





$$\frac{\partial s}{\partial t} = D\frac{\partial^2 s}{\partial x^2} - \mu E\frac{\partial s}{\partial x} - \frac{s}{\tau_s}$$

Diffusion Coefficient — Mobility — Relaxation Time

Need to first develop compact models for material properties: Cu, Al, and Si

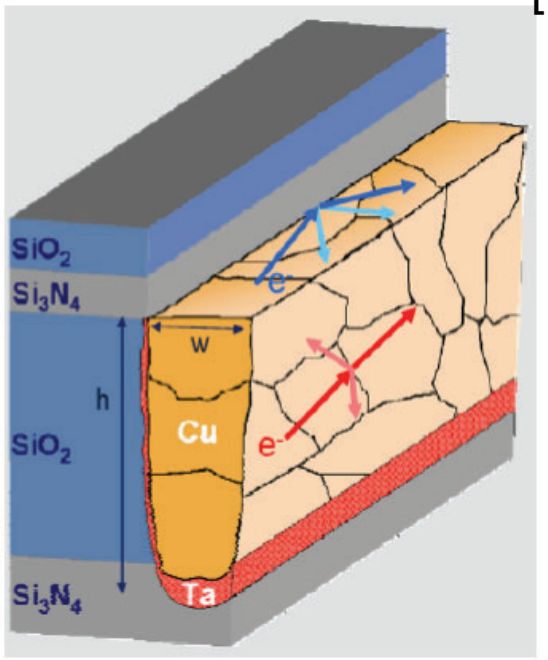
Power Dissipation:

$$P = RI^2$$

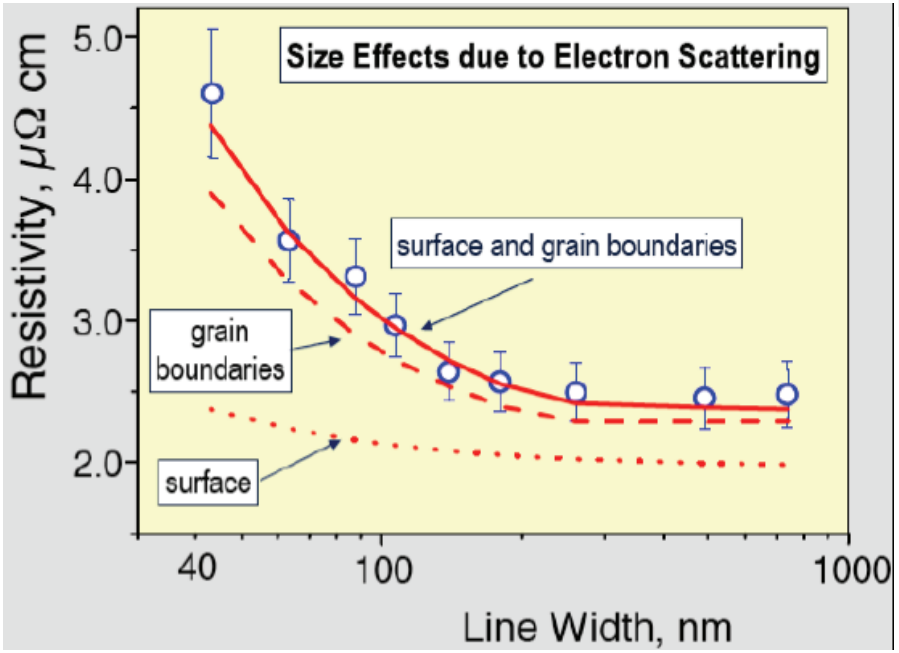
Resistivity

Scaling Metallic Wires

[1]



[1]



More scatterings at wire surfaces and grain boundaries.

Resistivity increases as cross-sectional dimensions scale.

[1] W. Steinhögl, et al., *Physical Rev. B,* Vol. 66, 075414 (2002).

Spin Transport Parameters in Metals

Grain-boundary **(R)** and sidewall **(p)** scatterings

↓ **Mayadas-Shatzkes Fuchs-Sondheimer**

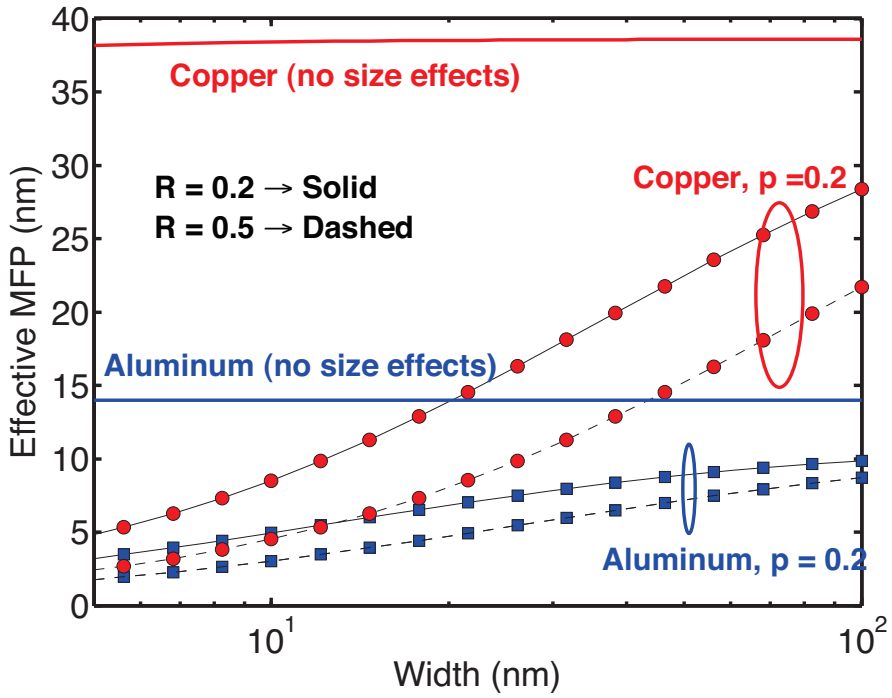
Effective resistivity & momentum relaxation time

↓ **Elliott-Yafet (EY) theory**

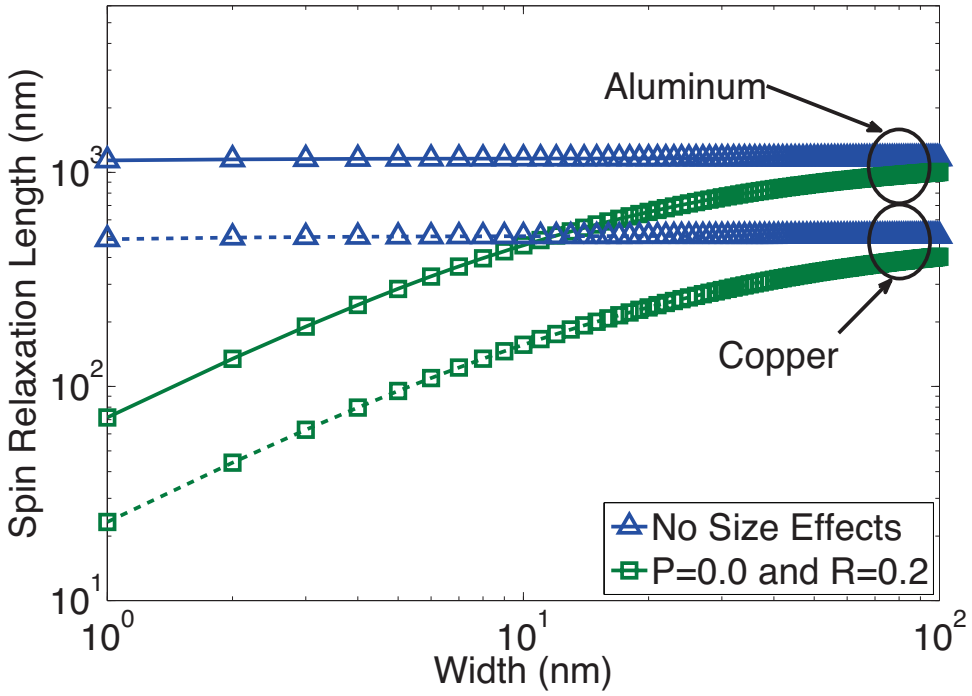
Spin-relaxation time

$$\tau_s \propto \tau_p$$

Effect of scaling and size effects on effective MFP in metals



Spin Relaxation in Cu and Al



$$L_s^{net} = \sqrt{\kappa}\,\frac{\lambda^d \lambda^{ph}}{\sqrt{\left(\lambda^d + \lambda^{ph}\right)\left(a^{ph}\lambda^d + a^d \lambda^{ph}\right)}}$$

$$\kappa = \frac{2}{3}\frac{E_{Fermi}}{m^* v_f^2}$$

$$a^d \approx 7\times10^{-4}$$

$$a^{ph} \approx 3\times10^{-3}$$

Size effects can lower spin diffusion length in narrow metallic wires substantially.

Sh. Rakheja et al., IEEE Trans. Electron Devices, Nov. 2013.

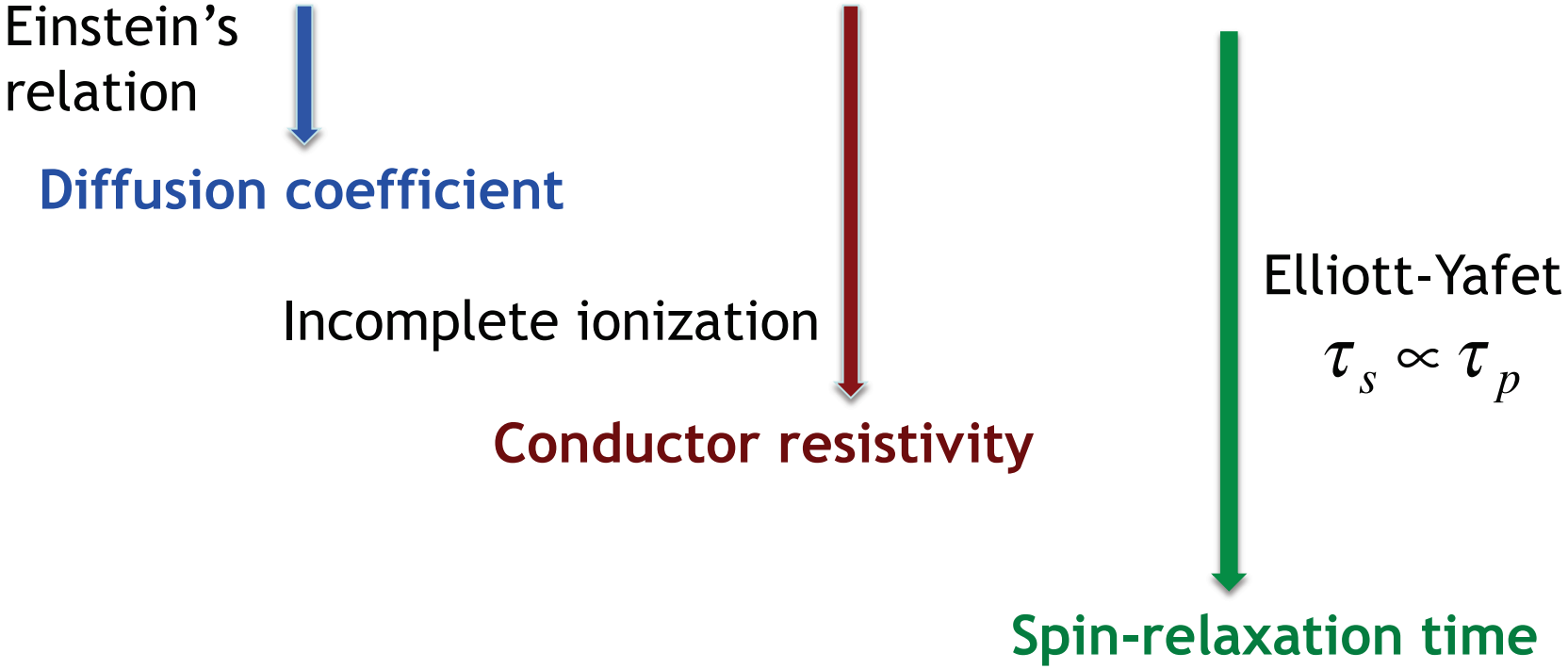
Calibration and Validation vs. Experiments

Copper							
Reference	Dimensions	$\rho(L.T.)$ $(\mu\Omega \cdot cm)$	$L_s^{net}(L.T.)$ (nm)	$\rho(R.T.)$ $(\mu\Omega \cdot cm)$	$L_s^{net}(R.T.)$ (nm)	a^d	a^{ph}
S. Garzon, 2005 [18]	$W/T = 100/54$	3.44	546	5.76	148	4.0×10^{-4}	5.7×10^{-3}
E. Villamor, 2013 [19]	$W/T = 200/70$	1.63	863	–	–	7.1×10^{-4}	–
E. Villamor, 2013 [19]	$W/T = 200/100$	1.26	1020	–	–	8.5×10^{-4}	–
E. Villamor, 2013 [20]	$W/T = 170/100$	1.7	860	3.5	380	6.5×10^{-4}	10^{-3}
H. Zou, 2010 [21]	$W/T = (150-200)/100$	1.3	1000	3.38	400	8.3×10^{-4}	10^{-3}
F. Jedema, 2001 [22] F. Jedema, 2003 [23]	cross-strip (50 nm thick)	1.41	1000	2.85	350	7.0×10^{-4}	1.8×10^{-3}
T. Kimura, 2006 [24], [25]	$W/T = 100/80$	1.14	1500	–	–	4.8×10^{-4}	–
T. Kimura, 2012 [26]	$W/T = 200/100$	2.5	1300	1.2	500	5.7×10^{-4}	10^{-3}
T. Kimura, 2008 [27]	$W/T = 220/320$	0.69	1000	2.35	400	2.9×10^{-3}	10^{-3}
H. Zou, 2012 [28]	$W/T = 100/72$	1.4	460	3.0	290	3.3×10^{-3}	5.4×10^{-4}

Sh. Rakheja et al., IEEE Trans. Electron Devices, Nov. 2013.

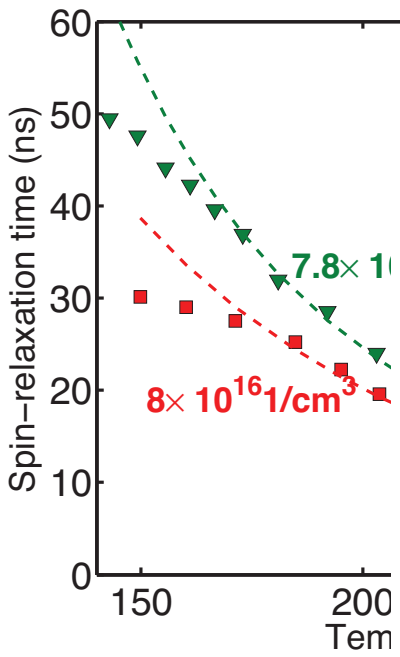
Spin Transport in Silicon

Klaassen semi-empirical mobility model[1]



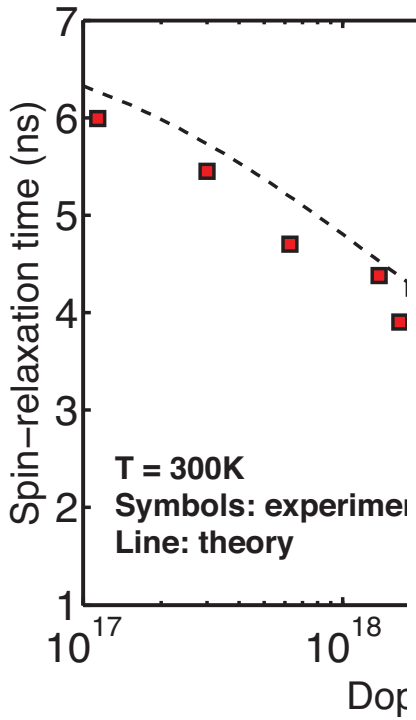
[1] D.B.M. Klaassen, Solid State Electronics, vol. 35, pp. 953– 959, July 1992.

Spin relaxation in silicon



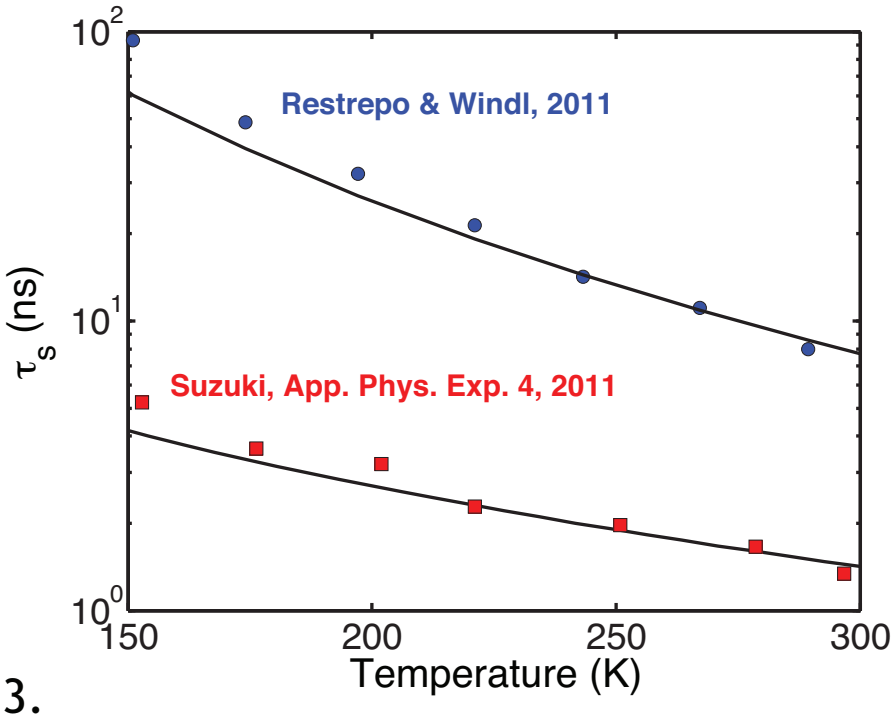
Symbols: Experiment
Line: Theory

Good match w/ experiments



error < 12 %

Good match w/ theory



IEEE Trans. Nanotechnology, Sept. 2013.

Summary of Spin Transport Parameters

Parameter	Cu (R=0.5, p=0.2)	Al (R=0.5, p=0.2)	Si (N_d = 1e18 cm^{-3})
D_s (cm^2/s)	18	22	7.5
μ_s (cm^2/Vs)	4	2.8	275
ρ_{eff} ($\mu\Omega.cm$)	18.7	12.5	2.79×10^4
L_s (μm)	0.071	0.102	1.4

Width = 7.5 nm

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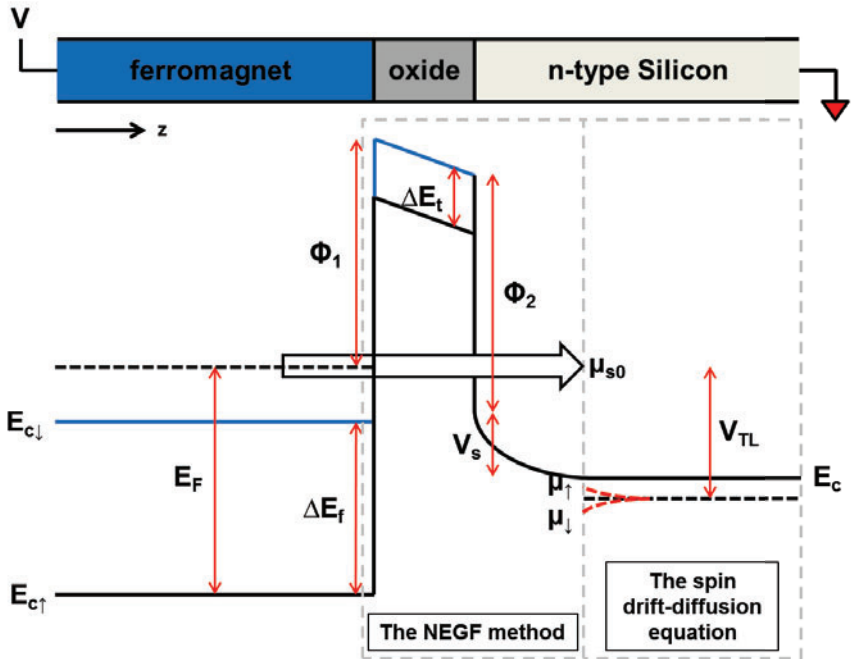
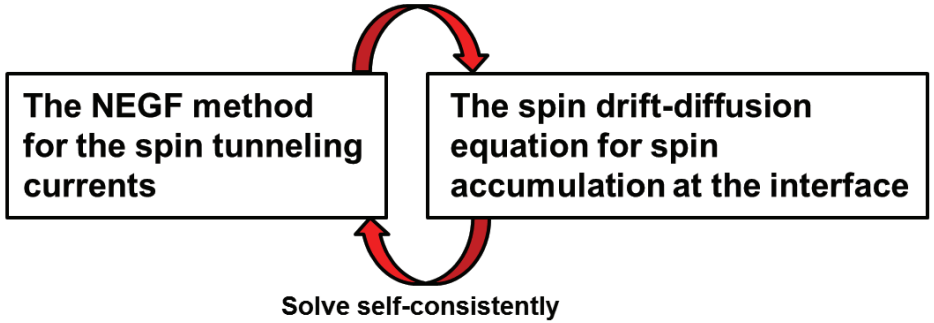
Spin Injection to Si: Methodology

The conducting electrons in F are modeled by majority and minority parabolic conduction bands.

The band bending at the Si interface is obtained by solving Poisson's equation under the Thomas-Fermi approximation.





S. Chang, et al., IEEE Trans. Magnetics (Si).
S. Chang, et al., IEEE Trans. Electron Devices (Cu).

Spin Torque Devices and Circuits

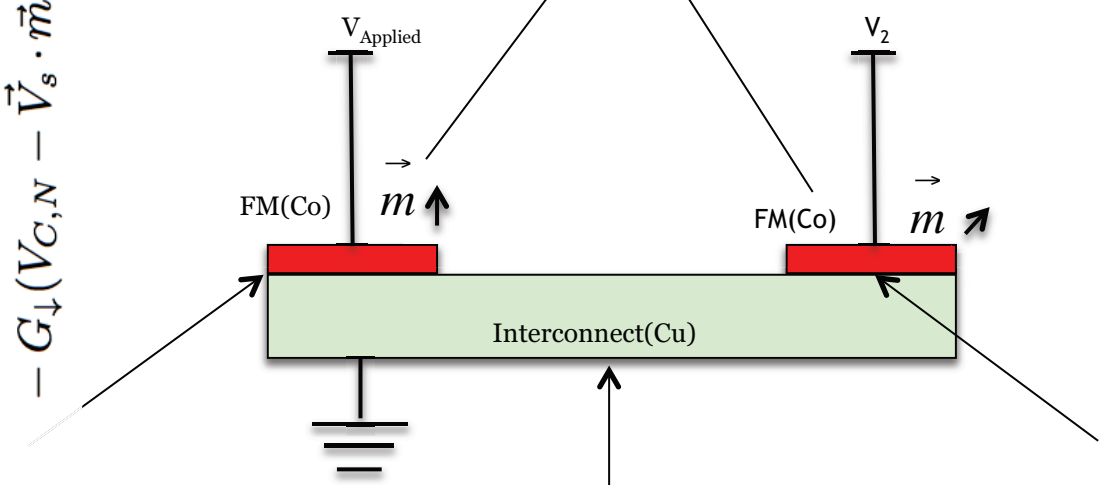
Spin Mixing Conductance

$$\vec{I}_{s,\perp} = 2\mathrm{Re}G_{\uparrow\downarrow}\vec{m}\times\left(\vec{V}_s\times\vec{m}\right)+2\mathrm{Im}G_{\uparrow\downarrow}\vec{V}_s\times\vec{m}.$$

$$\vec{I}_{s,\parallel} \equiv \vec{m}\cdot[G_{\uparrow}(V_{C,N}+\vec{V}_s\cdot\vec{m}-V_{C,F}) - G_{\downarrow}(V_{C,N}-\vec{V}_s\cdot\vec{m}-V_{C,F})],$$

Stochastic LLG for nanomagnet dynamic

$$\frac{d\vec{m}}{dt} = -\gamma\mu_0\left[\vec{m}\times\vec{H}_{eff}\right]+\alpha\left[\vec{m}\times\frac{d\vec{m}}{dt}\right]+\frac{\vec{I}_{S,\perp}}{qN_s}$$

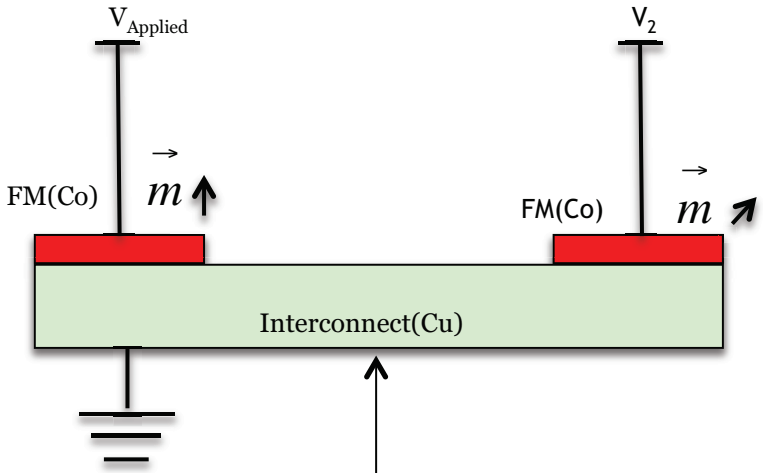


Spin Mixing Conductance

$$\frac{\partial s}{\partial t} = D\frac{\partial^2 s}{\partial x^2}-\mu E\frac{\partial s}{\partial x}-\frac{s}{\tau_s}$$

Spin Drift-Diffusion in non-magnetic channel

Spin Transport in Non-Magnetic Channel



$$\frac{\partial \vec{s}}{\partial t} = D\frac{\partial^2 \vec{s}}{\partial x^2} - \mu E\frac{\partial \vec{s}}{\partial x} - \frac{\vec{s}}{\tau_s}$$

Spin Drift-Diffusion in non-magnetic channel

The x Component of the Spin Transport

$$J_{s-x} = qD\frac{\partial s_x}{\partial x} + q\mu E s_x$$

x Spin current density

Diffusion

Drift

Spin Voltage

Electrochemical potential

Quantum Capacitance per unit volume

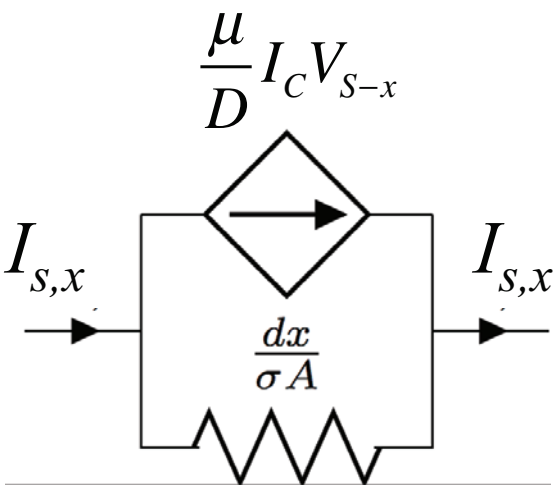
$$V_{s-x} \equiv \frac{\eta_{s-x}}{q} \longrightarrow s_x = \frac{C_Q V_{s-x}}{q}$$

$$D.C_Q = \sigma$$

$$J_{s-x} = \sigma\frac{\partial V_{s-x}}{\partial x} + \frac{\mu}{D}J_C V_{S-x}$$

Conductivity

Electrical Current density

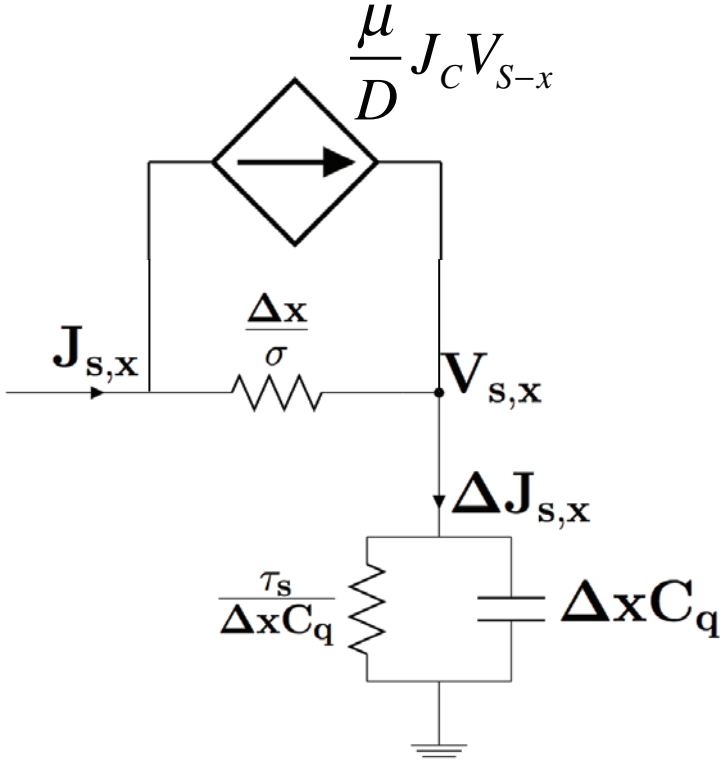


The x Component of the Spin Transport

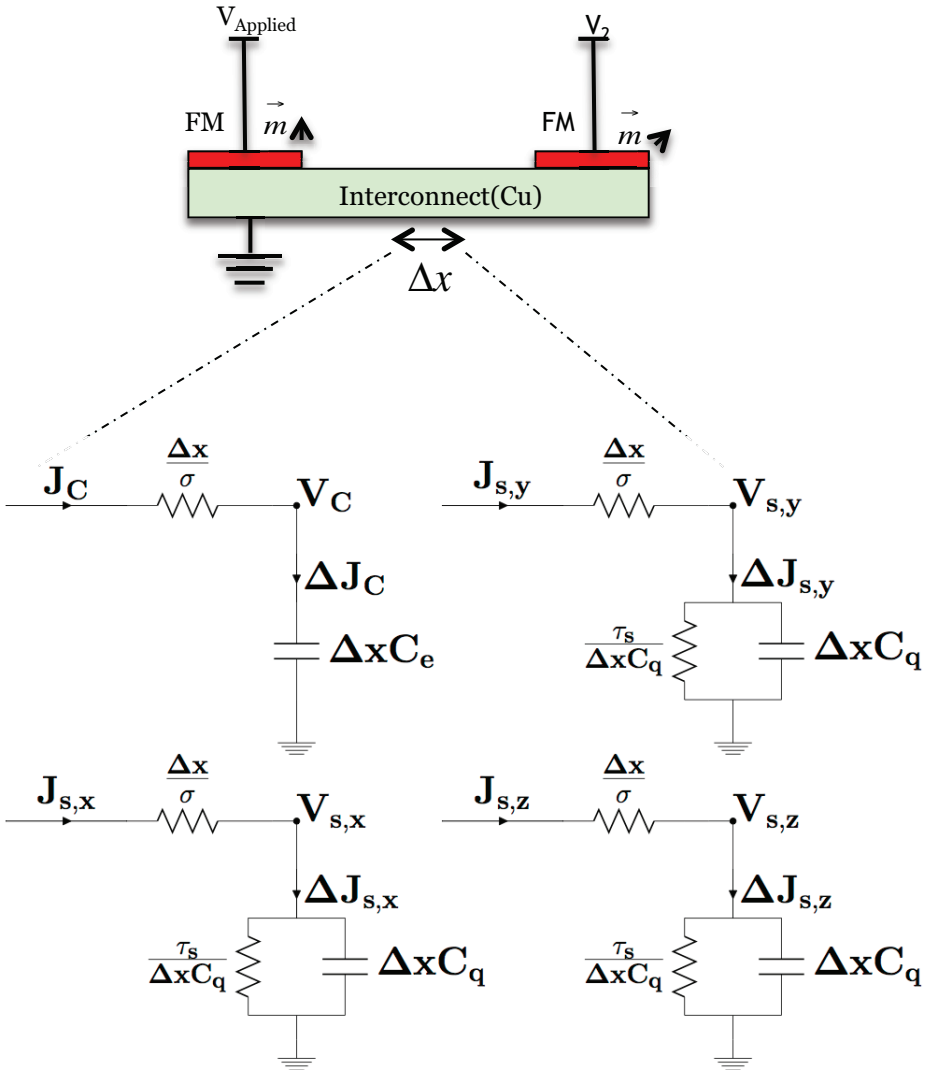
$$\frac{\partial s_x}{\partial t} = \frac{1}{q}\frac{\partial J_{s-x}}{\partial x} - \frac{s_x}{\tau_s}$$

$$s_x = \frac{C_Q V_{s-x}}{q}$$

$$\frac{\partial J_{s-x}}{\partial x} = \frac{\sigma}{D\tau_s} V_{s-x} + C_Q \frac{\partial V_{s-x}}{\partial t}$$

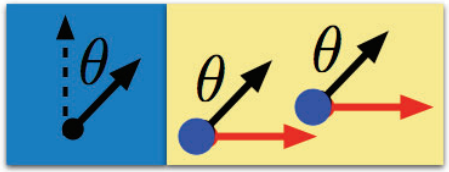


Complete Circuit: Non-Magnetic Metallic Channel

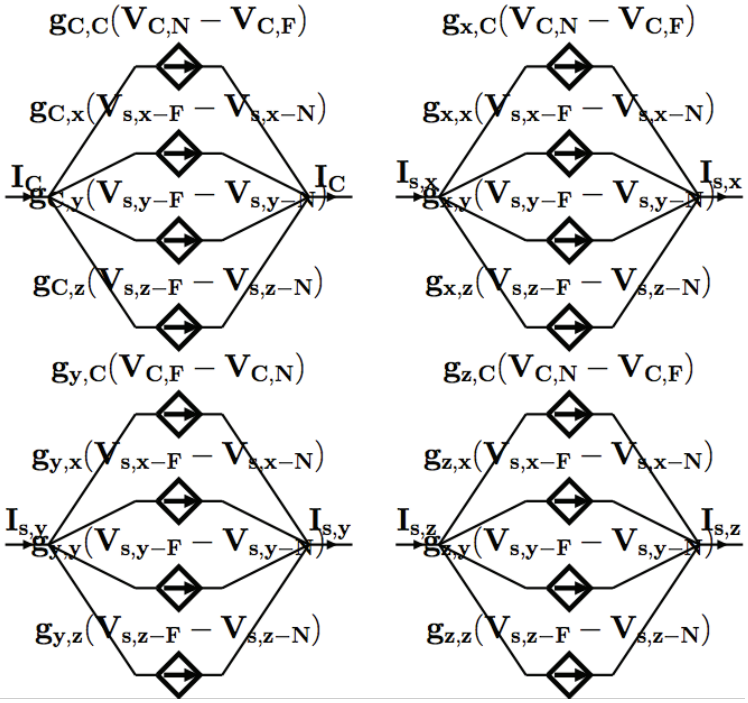


Magnet-Non Magnet Interface

$$\vec{I}_S = \begin{bmatrix} I_C \\ I_{S,x} \\ I_{S,y} \\ I_{S,z} \end{bmatrix} \qquad \vec{V}_S = \begin{bmatrix} V_C \\ V_{S,x} \\ V_{S,y} \\ V_{S,z} \end{bmatrix} \qquad \vec{I}_s = [G]\ \Delta\vec{V}_S \qquad \overline{G}_{\vec{m}} = \begin{bmatrix} g_{C,C} & g_{C,x} & g_{C,y} & g_{C,z} \\ g_{x,C} & g_{x,x} & g_{x,y} & g_{x,z} \\ g_{y,C} & g_{y,x} & g_{y,y} & g_{y,z} \\ g_{z,C} & g_{z,x} & g_{z,y} & g_{z,z} \end{bmatrix}$$



$$\begin{bmatrix} V_{C,F} \\ V_{S,x-F} \\ V_{S,y-F} \\ V_{S,z-F} \end{bmatrix} \qquad \begin{bmatrix} V_{C-N} \\ V_{S,x-N} \\ V_{S,y-N} \\ V_{S,z-N} \end{bmatrix}$$



S. Manipatruni, et al., IEEE Trans. Circuits and Systems, Dec. 2012.

Nanomagnet Dynamics

$$\frac{d\vec{m}}{dt} = -\gamma\mu_0\left[\vec{m}\times\vec{H}_{eff}\right] + \alpha\left[\vec{m}\times\frac{d\vec{m}}{dt}\right] + \frac{\vec{I}_{S,\perp}}{qN_s}$$

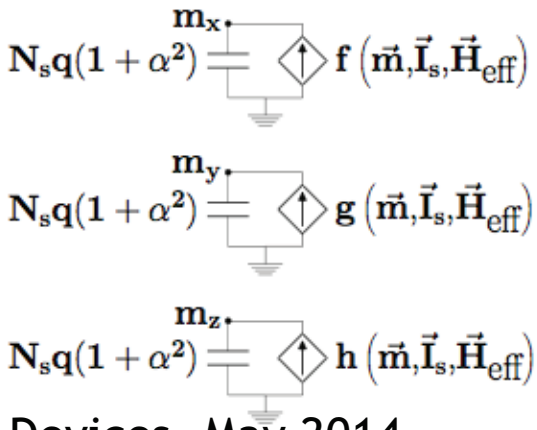
$\vec{m}$

$$N_s q(1+\alpha^2)\frac{dm_x}{dt} = f(m_x, m_y, m_z, V_{S,x}, V_{S,y}, V_{S,z}, H_{eff,x}, H_{eff,y}, H_{eff,z})$$

$$N_s q(1+\alpha^2)\frac{dm_y}{dt} = f(m_x, m_y, m_z, V_{S,x}, V_{S,y}, V_{S,z}, H_{eff,x}, H_{eff,y}, H_{eff,z})$$

$$N_s q(1+\alpha^2)\frac{dm_z}{dt} = f(m_x, m_y, m_z, V_{S,x}, V_{S,y}, V_{S,z}, H_{eff,x}, H_{eff,y}, H_{eff,z})$$

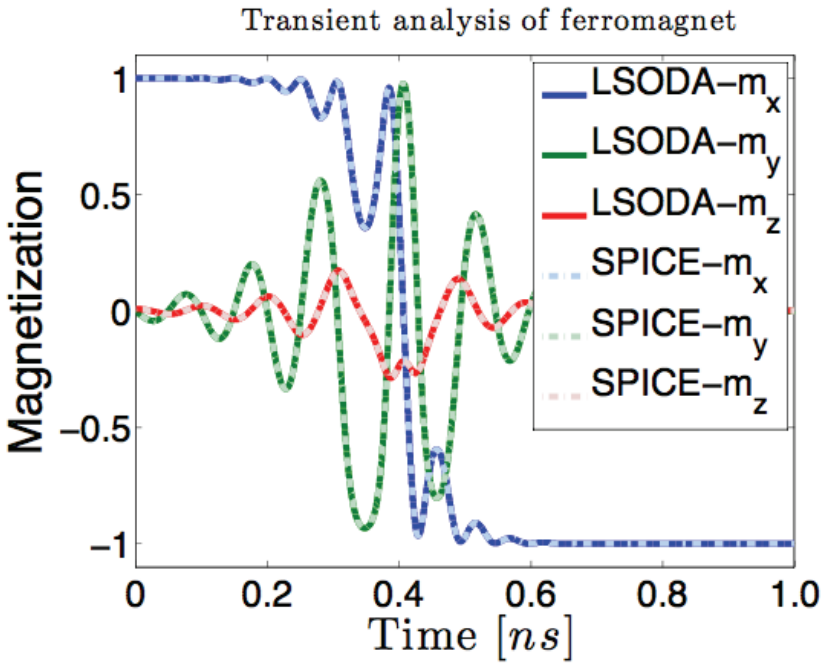
$$C\frac{dV(t)}{dt} = i(t)$$



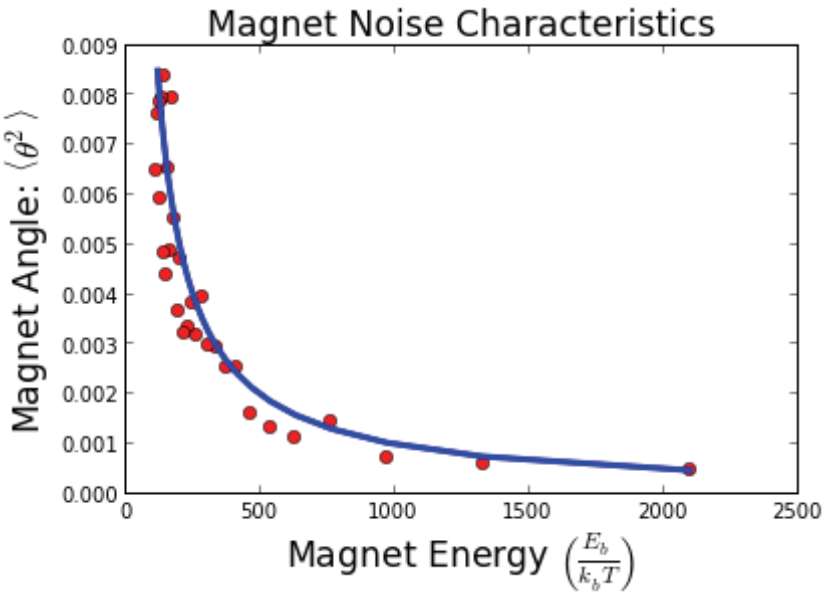
Ph. Bonhomme, et all. IEEE Trans. Electron Devices, May 2014.

Nanomagnet Circuit: Validation

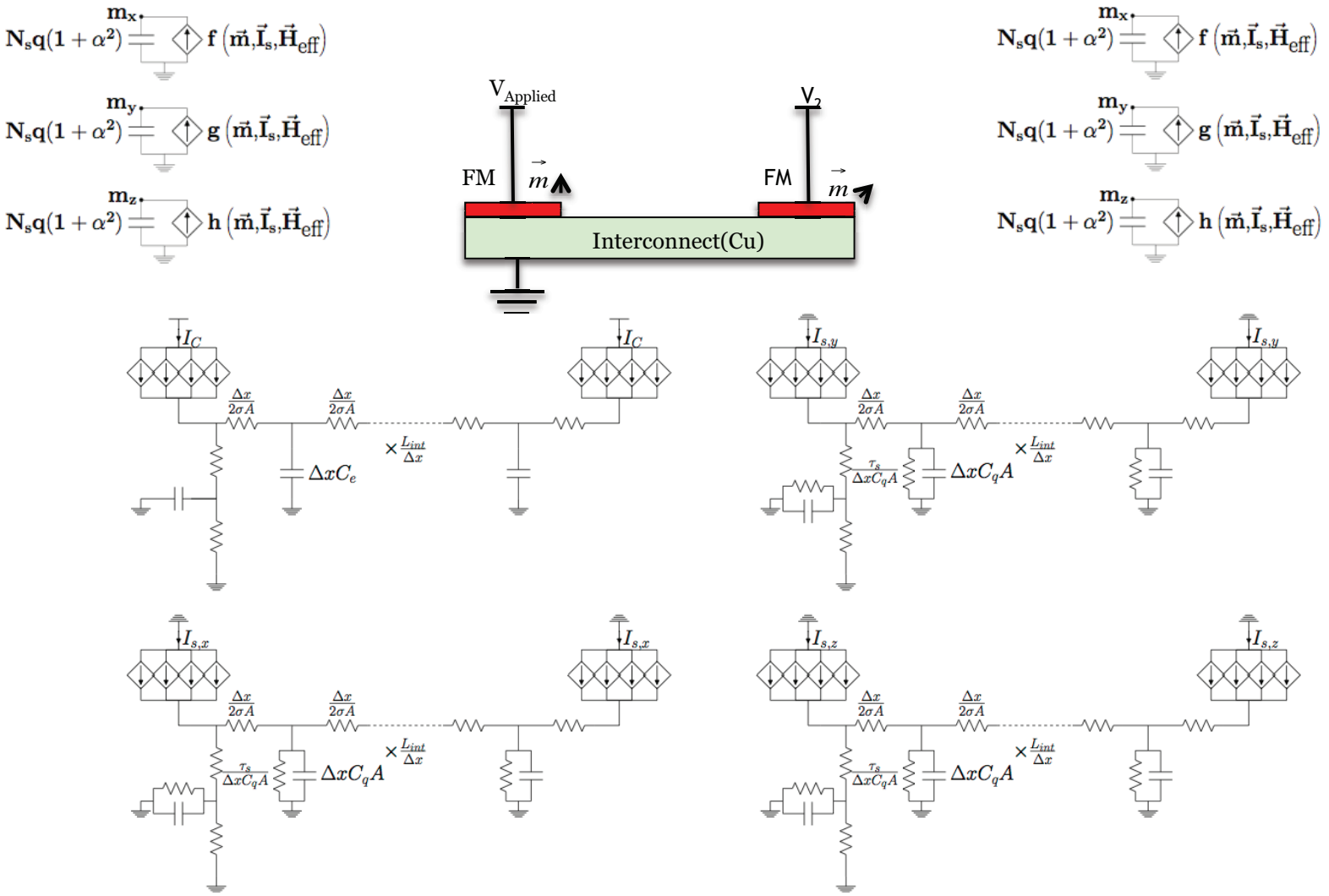
- **Transient Simulation**
  - SPICE vs. Numerical



- **Thermal Noise**



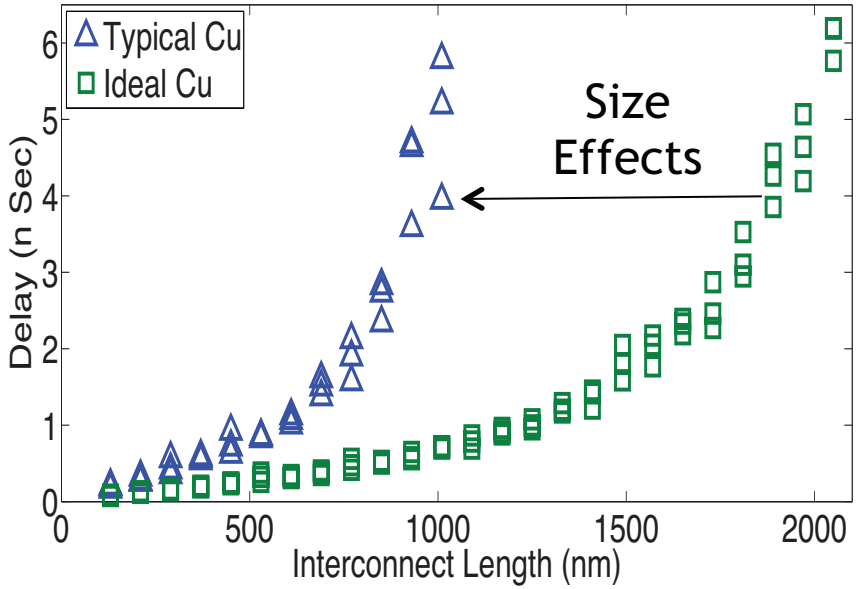
Complete Circuit Model

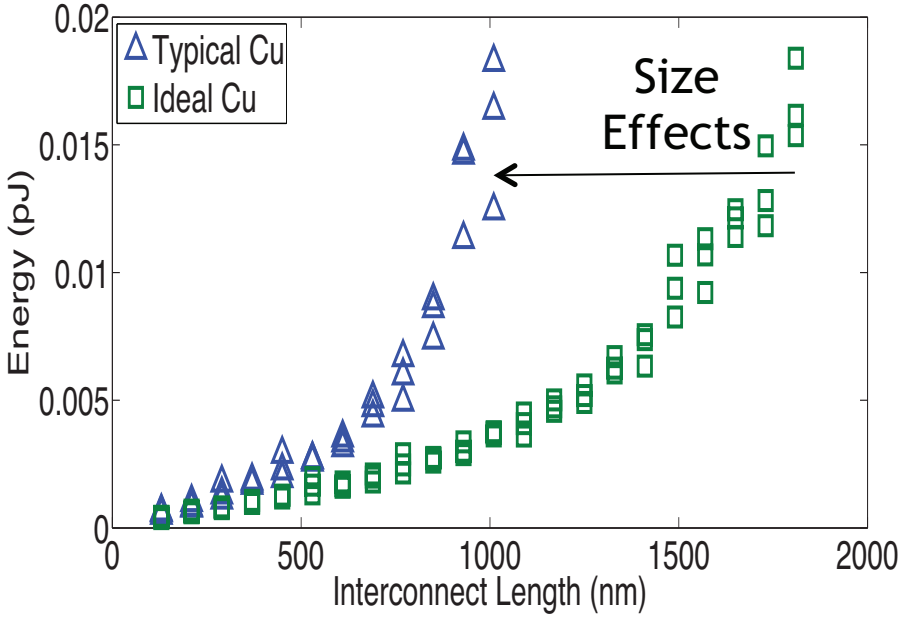


Ph. Bonhomme, et all. IEEE Trans. Electron Devices, May 2014.

Delay and Energy-per-bit vs. Length

Typical:	*Ideal*:	Interconnect:	Magnet Size
R =0.2	R =0.0	W_{int} =40 nm	$a = 80nm$
P=0	P=1	T_{int}/W_{int}=2.0	$b = 40nm$
			$c = 3nm$

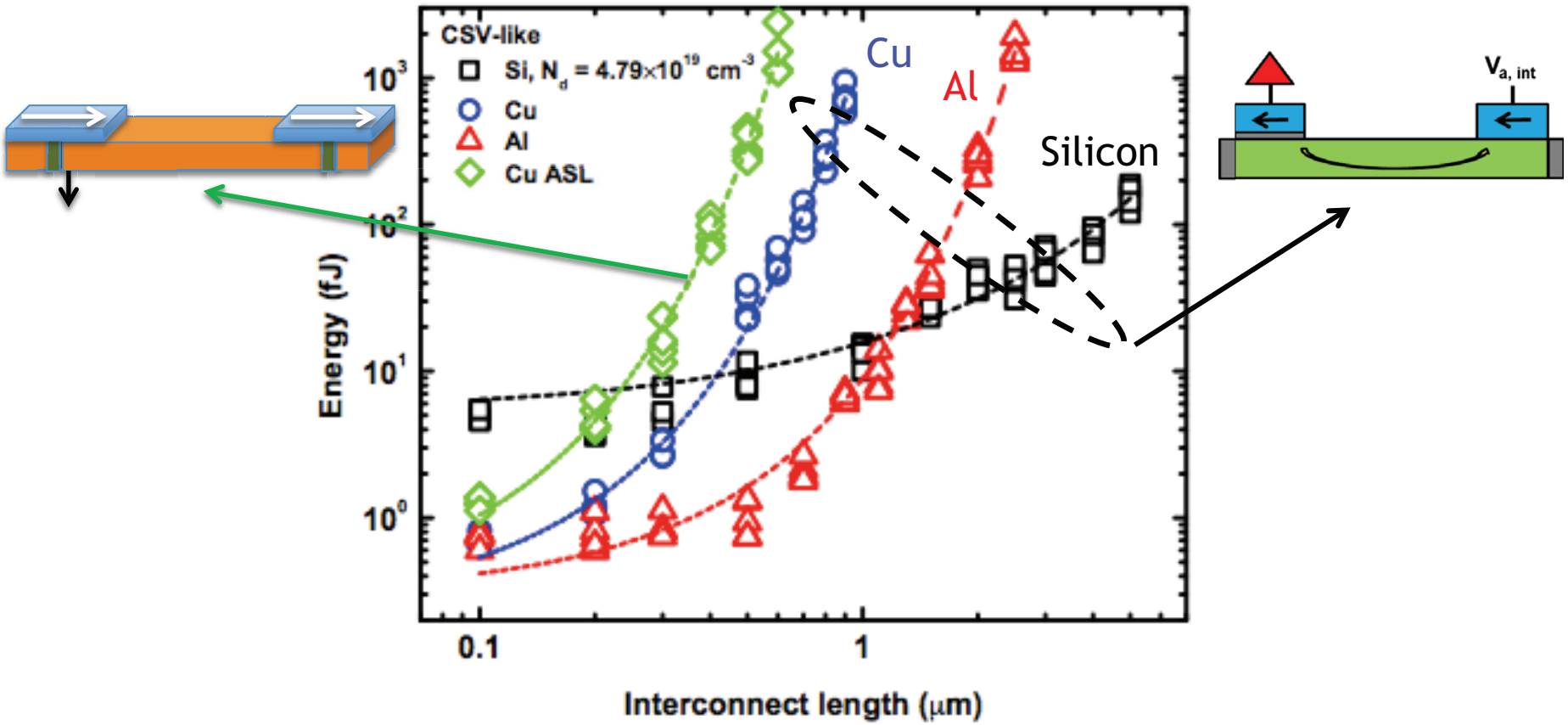




Size effects increase delay and energy in interconnects substantially.

Spin interconnects can be used only for very short lengths.

Comparing various Options @ Constant Delay



Conventional Spin Valve devices/interconnects are more energy efficient.

Metallic channels are better for shorter lengths and Si for longer lengths.

Outline

- Introduction
- Spin Drift/Diffusion Devices and Interconnects
  - Materials
  - Devices
  - Circuits & systems
- Spin Wave Circuits
- Conclusions

Overview

It is very difficult to compete with CMOS in traditional Boolean circuits.

Need to search for non-traditional circuits where beyond-CMOS devices can perform well:

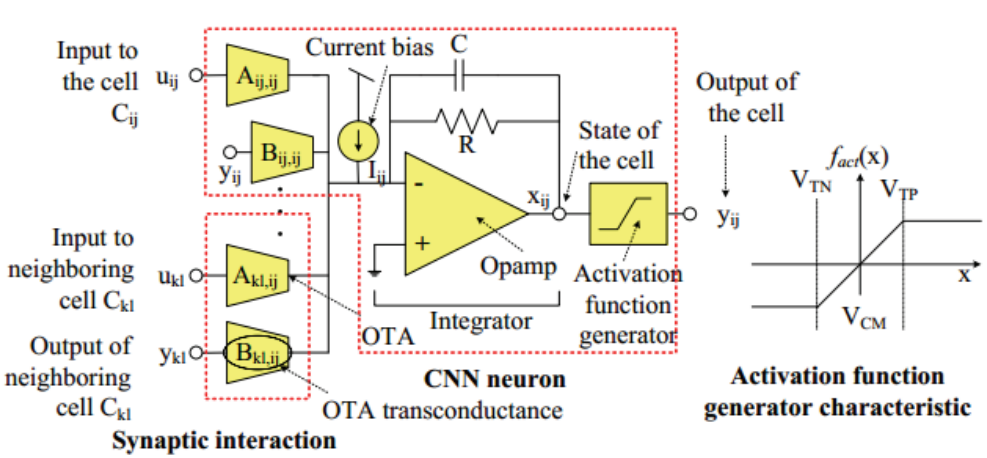
Cellular neural network is one possible candidate and was shown to provide better energy efficiency for specific tasks, such as the image processing, associative memory, and target tracking.

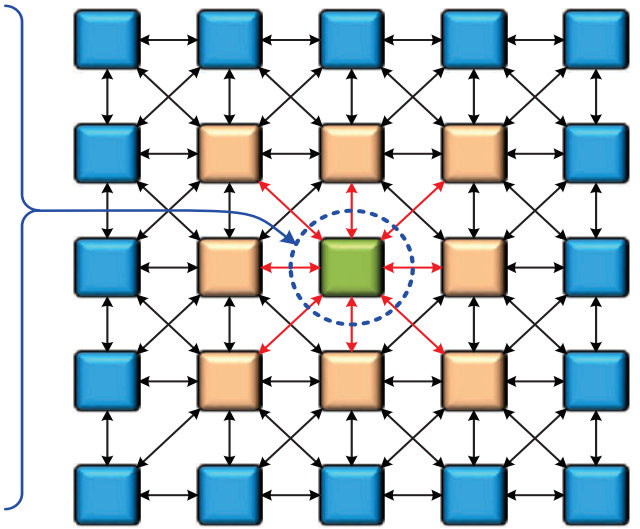
It can be implemented in a wide range of charge- and spin-based devices.

CNN Dynamic and Implementation

- **Illustrations of a CNN implemented with CMOS synapses and neurons**

$$C\frac{dV(x_{ij})}{dt} = -\frac{V(x_{ij})}{R} + \sum_{kl\in S_{ij}} A_{kl,ij} f_{act}(V(x_{ij})) + \sum_{kl\in S_{ij}} B_{kl,ij} V(u_{kl}) + I_{ij},$$





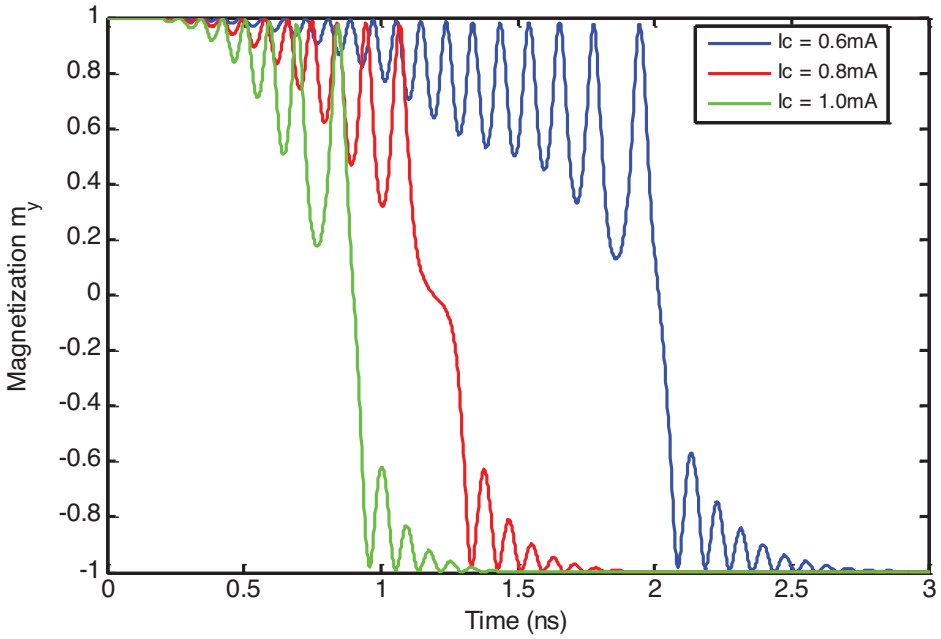
CMOS Implementation with Opamp and OTA

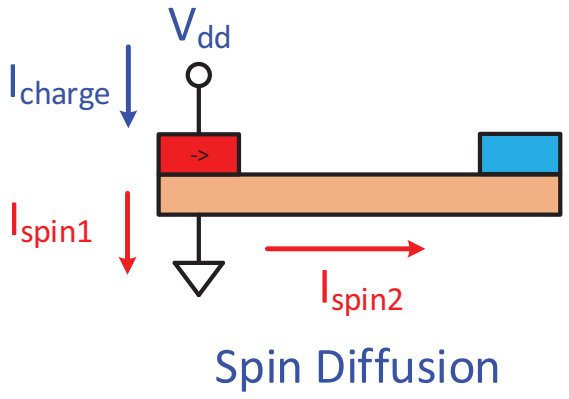
A. Trivedi, et al., "Application of Silicon-Germanium Source Tunnel-FET to Enable Ultralow Power Cellular Neural Network-Based Associative Memory ", IEEE TED, vol. 61, No.11, 2015.

Spintronic CNN Implementation

- **Using All-spin logic device as the building block**

$$\frac{d\vec{m}}{dt} = -\gamma\mu_0\left[\vec{m}\times\vec{H}_{eff}\right] + \alpha\left[\vec{m}\times\frac{d\vec{m}}{dt}\right] + \frac{\vec{I}_{S,\perp}}{qN_s}$$



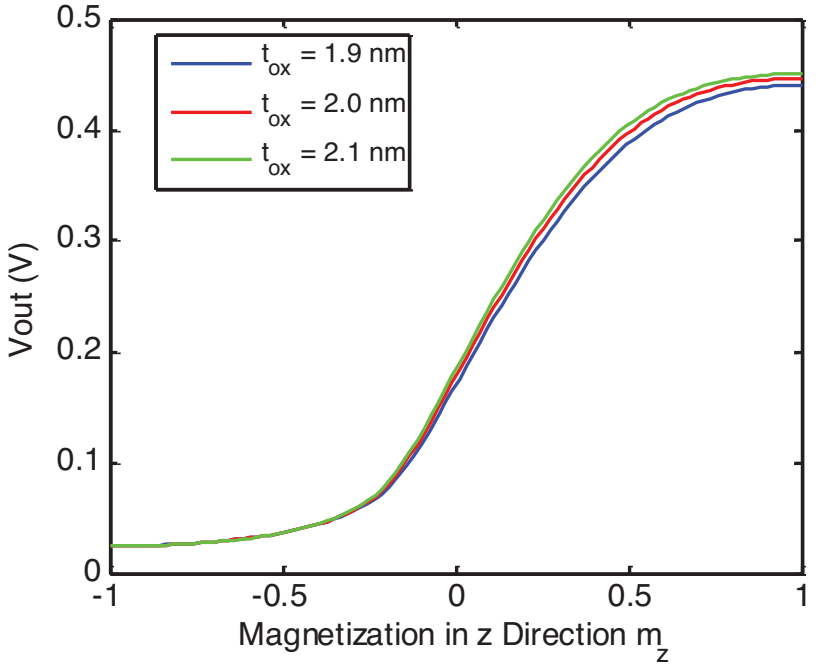


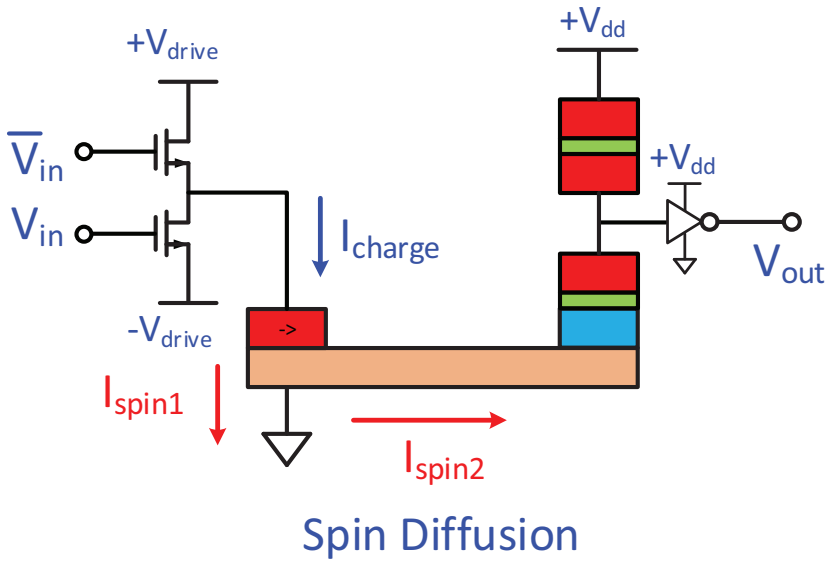
- The output magnet switches slower as the input current decreases, acting as an integrator.

Spintronic CNN Implementation

- **Using All-spin logic device as the building block**

$$\frac{d\vec{m}}{dt} = -\gamma\mu_0\left[\vec{m}\times\vec{H}_{eff}\right] + \alpha\left[\vec{m}\times\frac{d\vec{m}}{dt}\right] + \frac{\vec{I}_{S,\perp}}{qN_s}$$



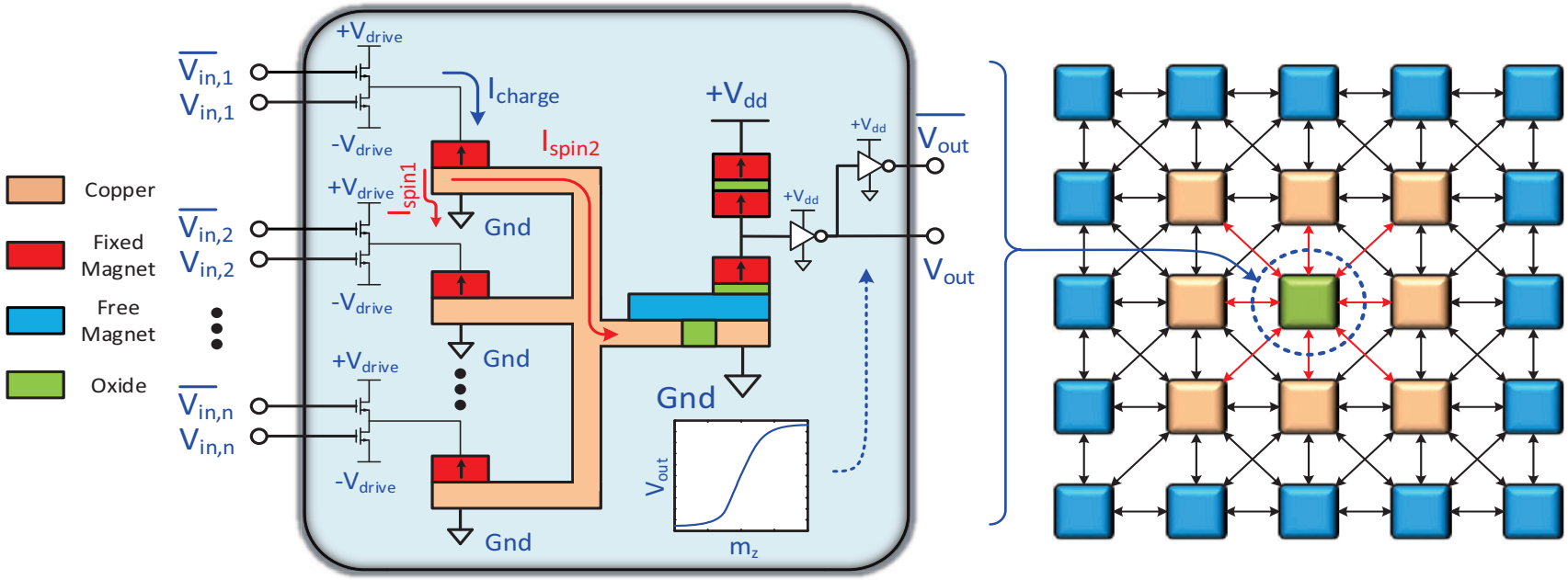


- The output magnet is sensed by using two MTJs and one inverters.
- MTJs are matched to tolerate the process variation.

Spintronic CNN Implementation

- **Illustrations of a CNN implemented with magnetic synapses and neurons**

$$\frac{d\vec{m}}{dt} = -\gamma\mu_0\left[\vec{m}\times\vec{H}_{eff}\right] + \alpha\left[\vec{m}\times\frac{d\vec{m}}{dt}\right] + \frac{\vec{I}_{S,\perp}}{qN_s}$$

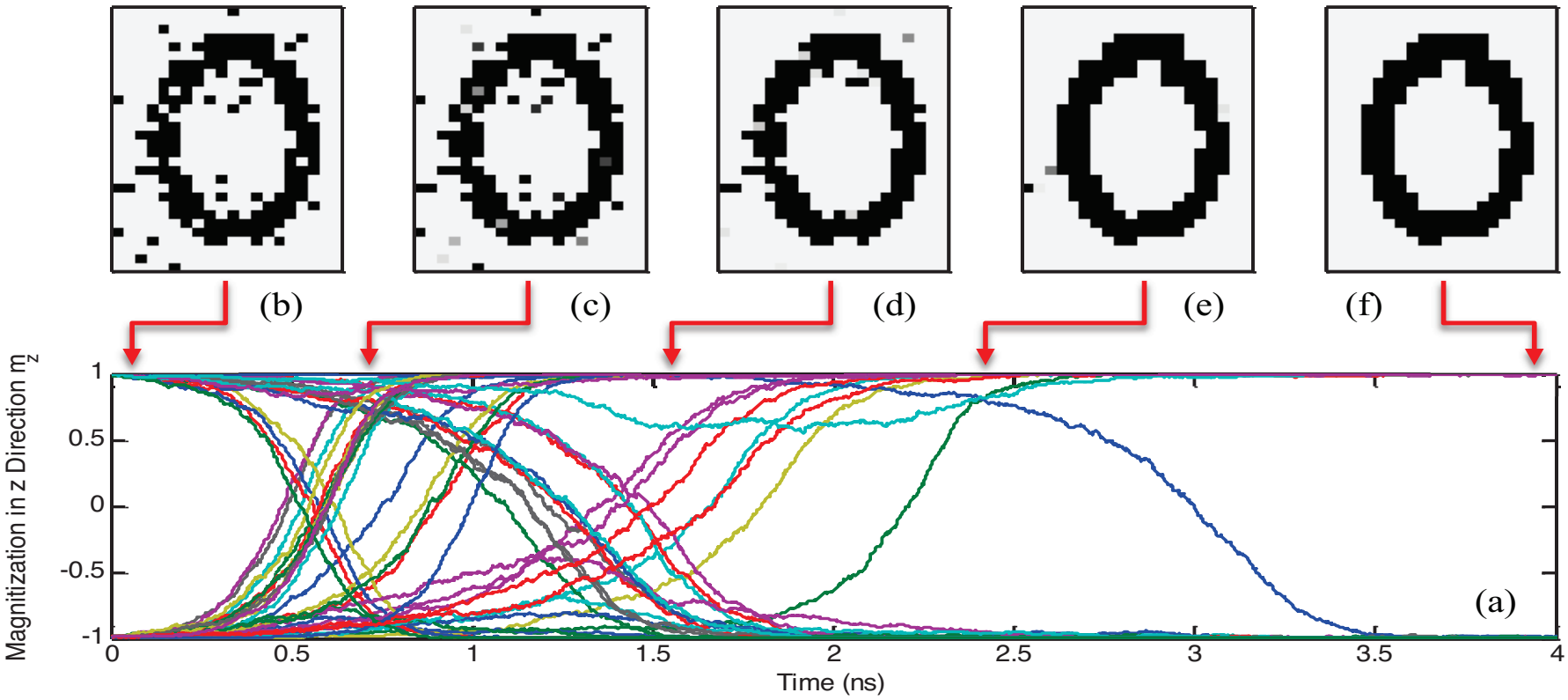


- **Other possible spin-torque transfer mechanisms to implement CNN are giant spin hall effect and domain wall motion.**

C. Pan and A. Naeemi, arXiv:1604.04584v1

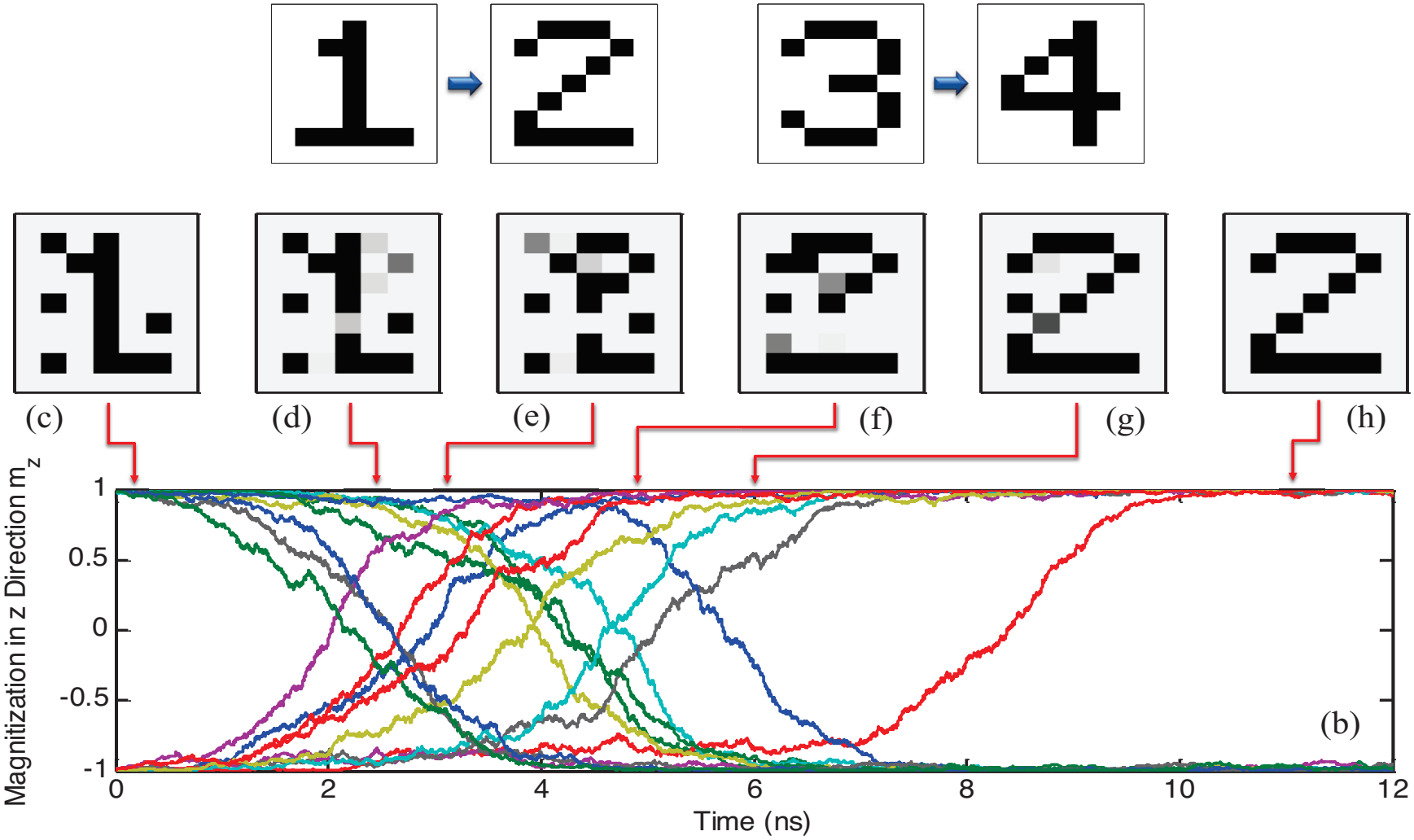
Noise Filtering

- Functional demonstration of a noise filtering application



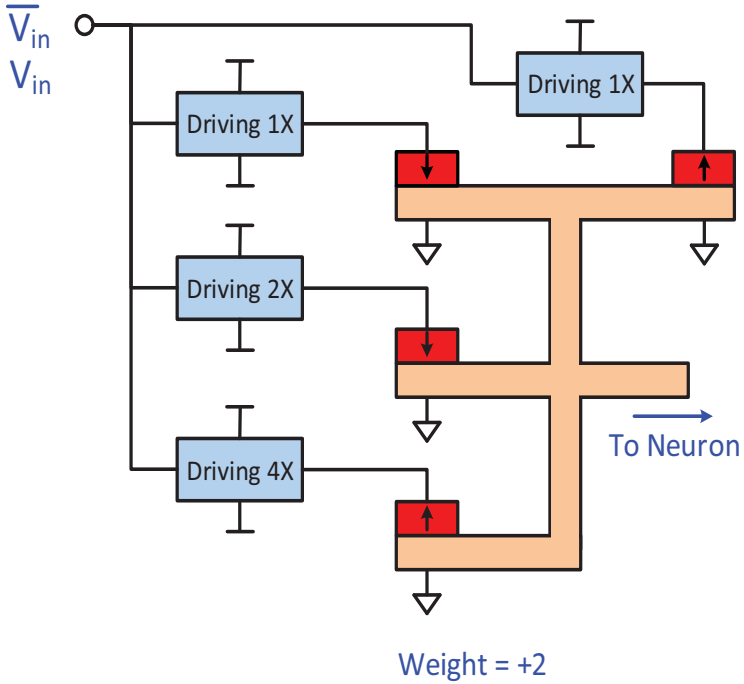
- Thermal noise has been included in all simulations.

Associative Memory Application



Spintronic CNN Implementation

- A magnetic synapse that has weight that is digitally programmable

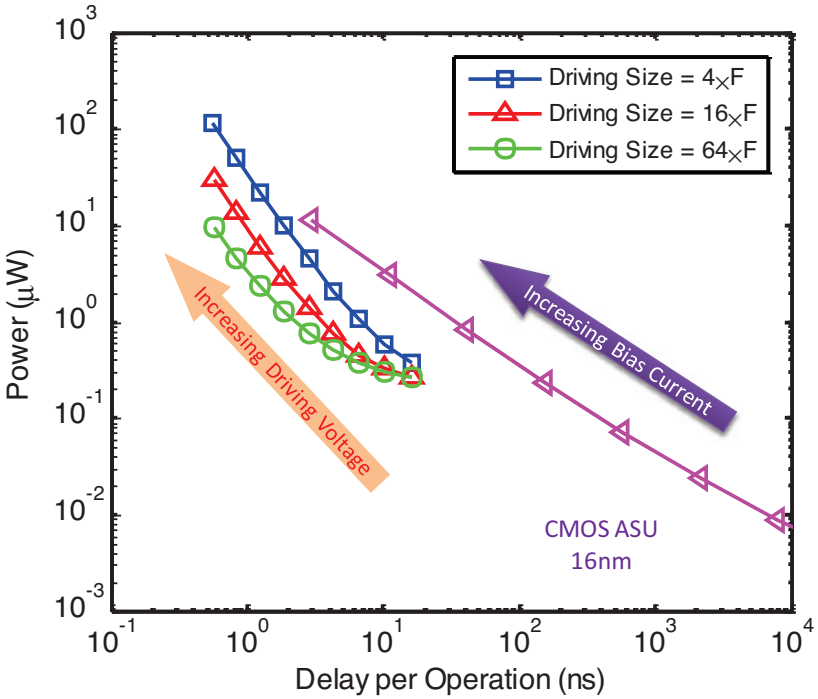


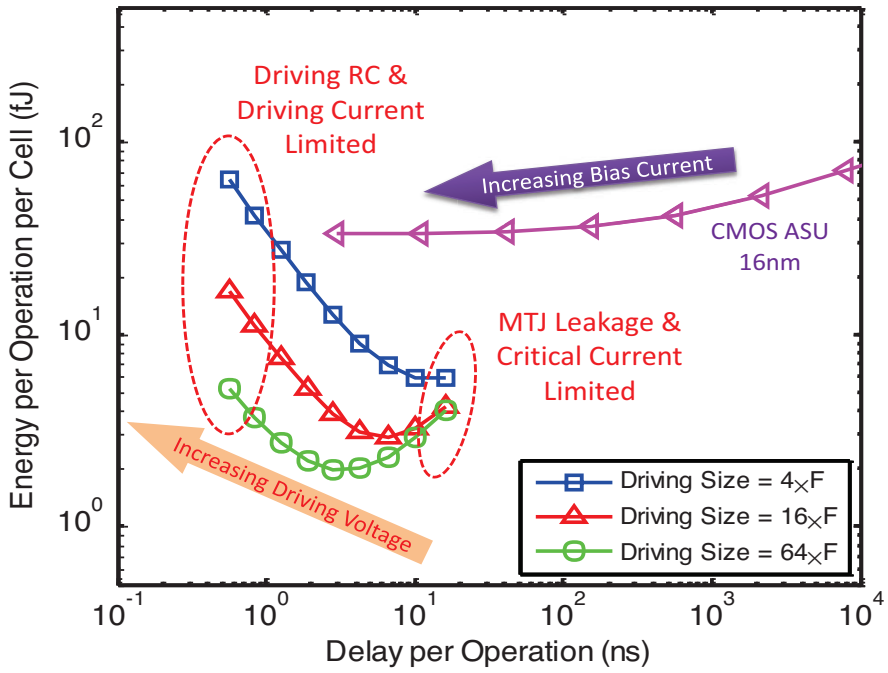
1X	1X	2X	4X	Weight
↑	↑	↑	↑	+8
↑	↓	↑	↑	+6
↑	↑	↓	↑	+4
↑	↓	↓	↑	+2
↓	↓	↓	↑	0
↓	↑	↑	↓	-2
↓	↓	↑	↓	-4
↓	↑	↓	↓	-6
↓	↓	↓	↓	-8

- To program the magnets, an extra layer of fixed magnet is placed on top of the input magnets.

Energy-Delay Benchmarking

- Performance comparison between spintronic and CMOS CNNs



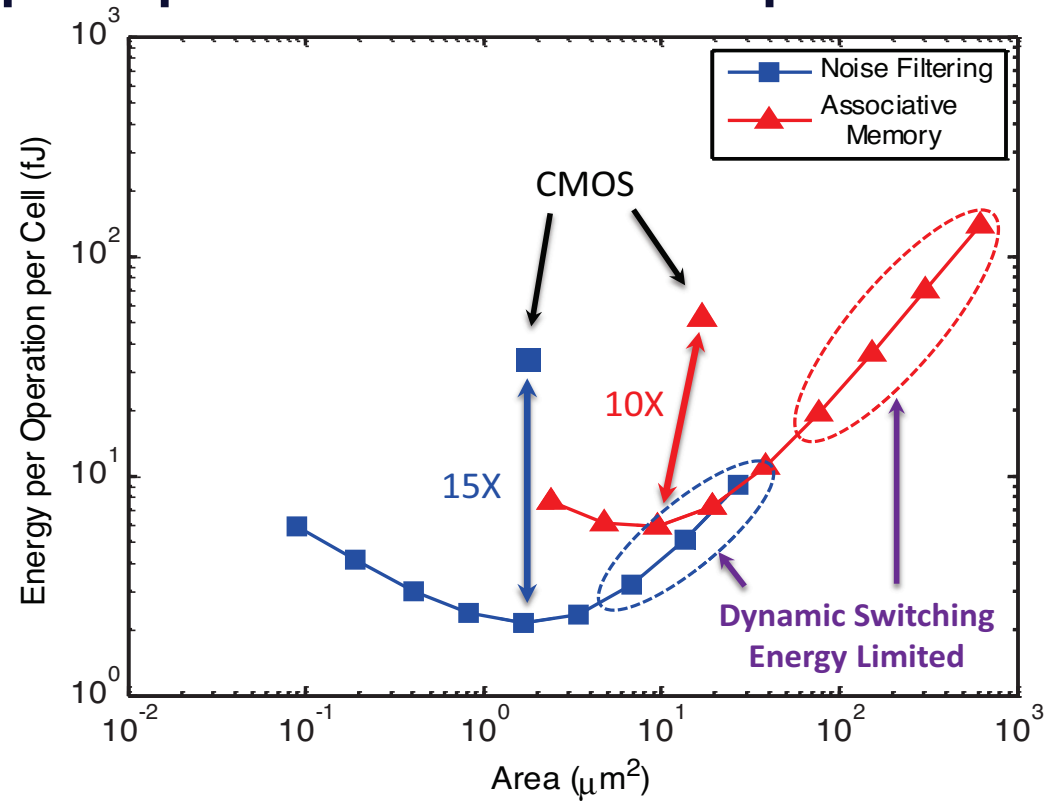


- For the spintronic CNN, an optimal driving supply voltage exists to minimize the energy for a given driving size.

C. Pan and A. Naeemi, arXiv:1604.04584v1

Area-Energy Trade-offs

- Energy per operation versus footprint area



- A larger driving size of the inverter reduces the energy dissipation at the cost of increasing the overall footprint area.

C. Pan and A. Naeemi, arXiv:1604.04584v1

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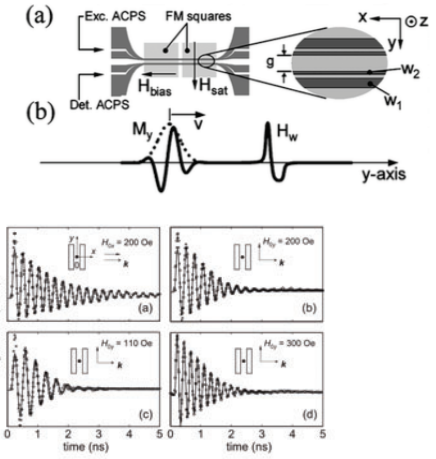
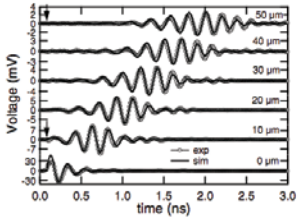
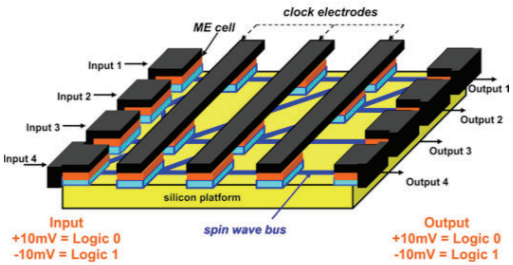
Recent Advancements: Spin Wave Excitation

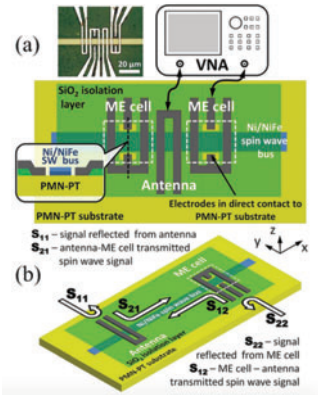




Oersted field (antenna)

Covington et al.
Z. Liu et al.

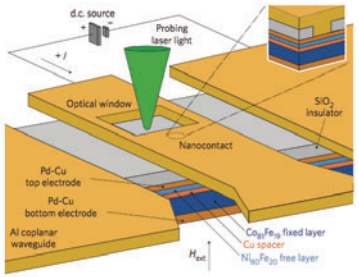




Magneto-electric effect

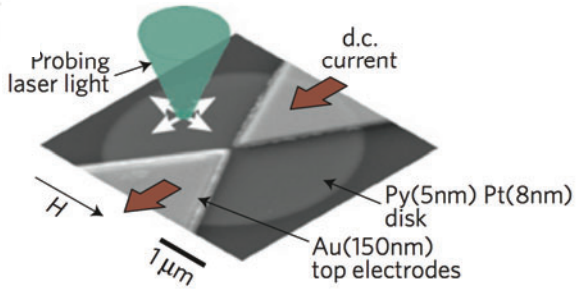
A. Khitun et al.

S. Cherepov, et al.



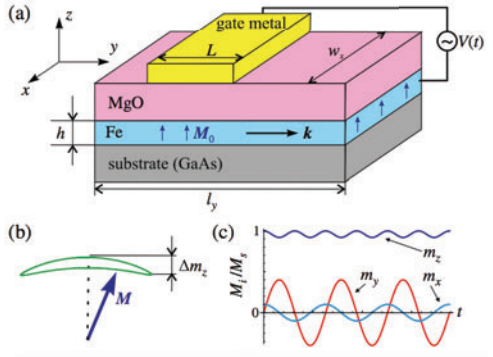
Spin torque

M. Madami et al.
V. E. Demidov et al.

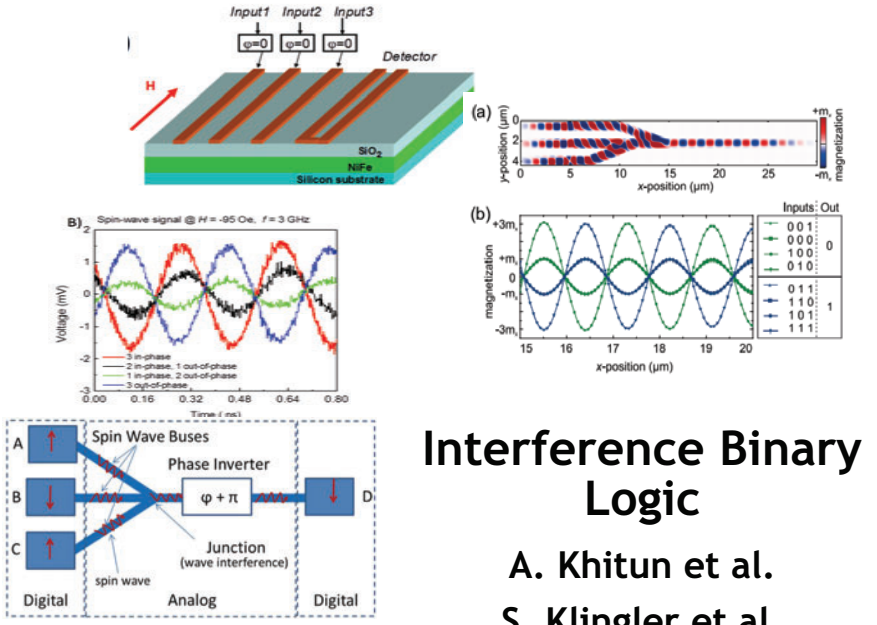


Parametric excitation

R. Verba, et al.



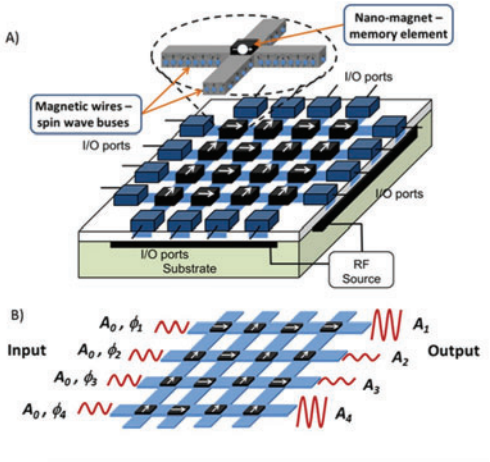
Recent Advancements: Spin Wave Logic



Interference Binary Logic

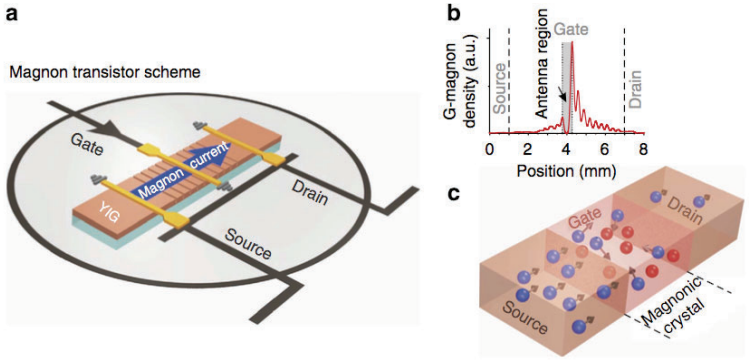
A. Khitun et al.

S. Klingler et al.



Magnonic holographic memory

F. Gertz et al.



Magnonic transistor

A. V. Chumak et al.

Issues not Considered/Addressed Before

- Spinwave signals are weak and attenuate fast:
  - Very few stages can be cascaded.
  - Detection needs very sensitive sense amplifiers
  - Frequent signal conversion takes energy and area

- Unidirectional operation or Non-reciprocity
  - An ME cell generates spinwaves that propagate in both directions
  - Need to make sure input determines the output not the other way around.

- Nonvolatility
  - One attractive feature of spintronic/magnetic circuits is their non-volatility.
  - Spin waves are volatile but magnets are nonvolatile.
  - Need memory elements

- Crosstalk noise
  - Not been modeled/considered
  - May limit the density and bandwidth

Requirements

1. Electrical signals must be converted to spinewave signals
2. Many stages of logic are performed in the spinwave domain
3. Unidirectional signal propagation is guaranteed.
4. The end result is easily converted back to electrical signals.

Assumptions/Choices:

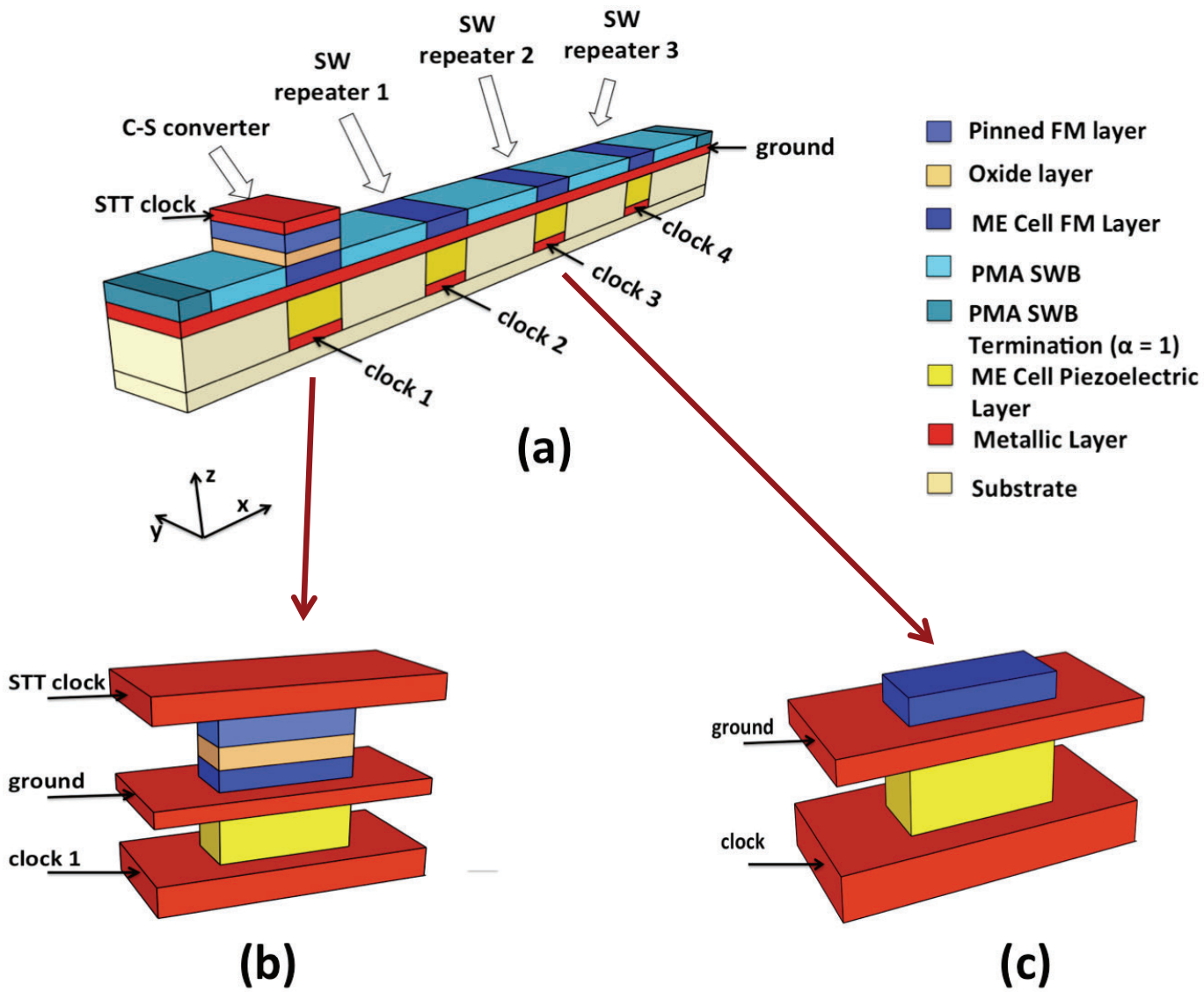
The spinwave logic complements CMOS circuits and is compatible with them.

Information is encoded in the phase of spin waves.

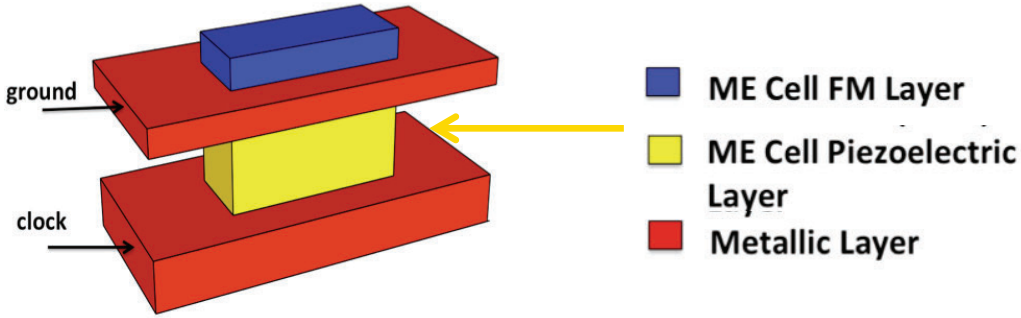
It is desired to have a non volatile spinwave logic.

For simplicity, start with an interconnect and copy/inverter logic functions.

Clocked Cascaded Spin Wave Devices

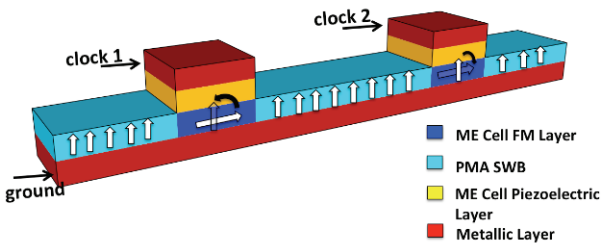


Basic Element



The Pz layer applies strain on the free FM to change the easy axis from in plane to out of plane.

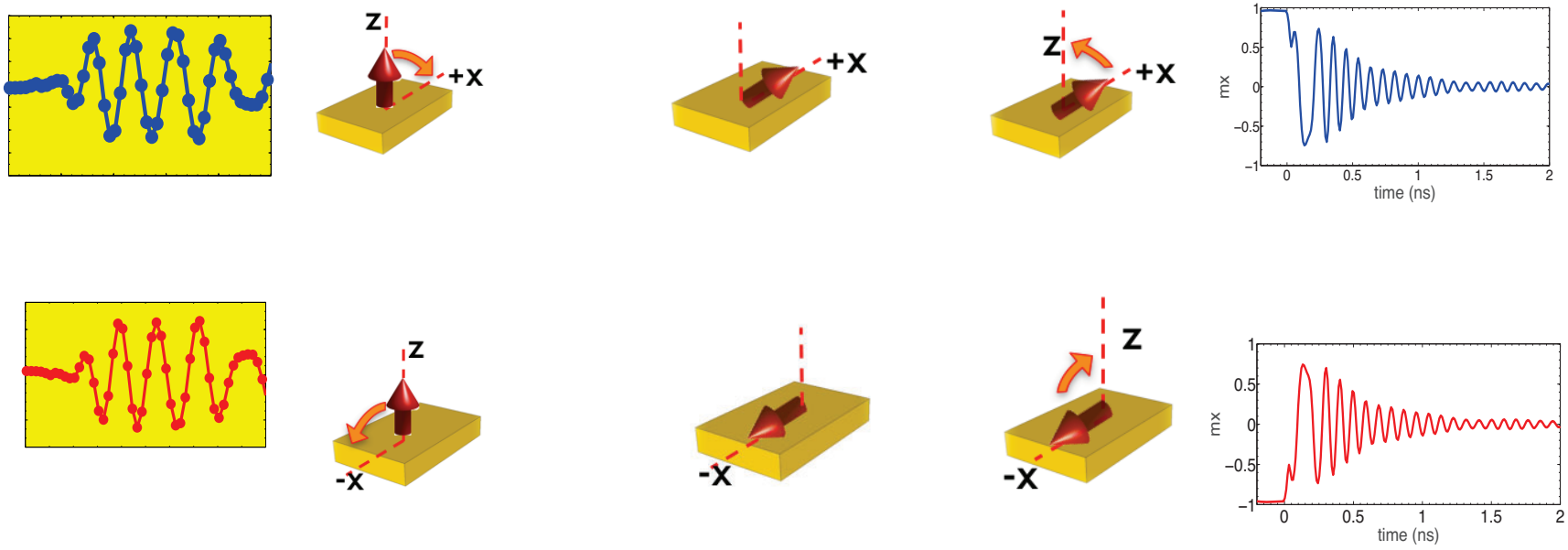
Non-Volatile SWD (Spin Wave Devices)



Write

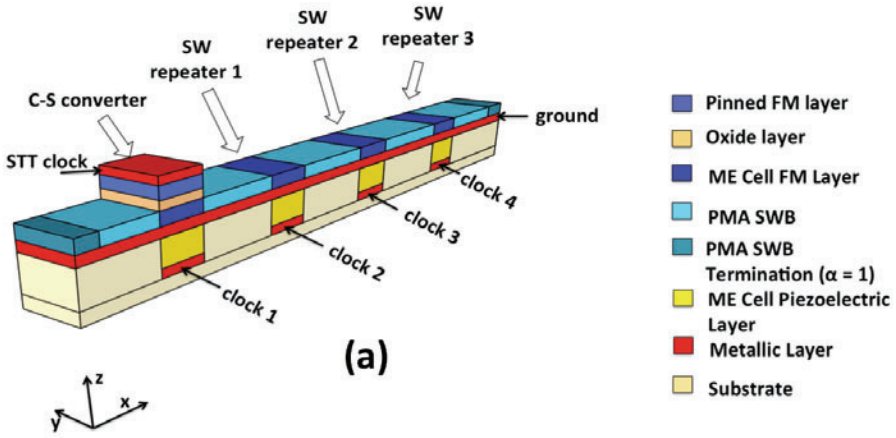
State Variable

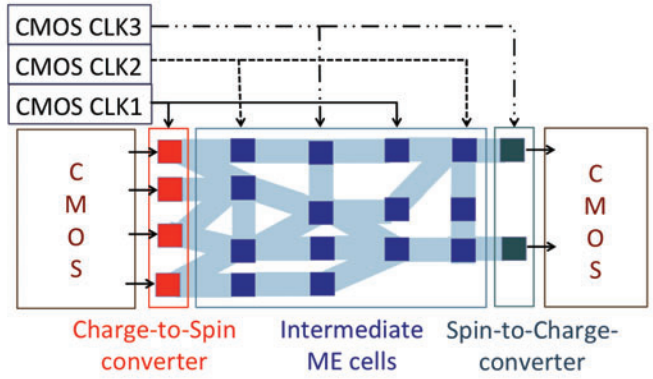
Read



S. Dutta, et al., Nature Scientific Report, **5**, Article number: 9861 (2015)

Interface with CMOS

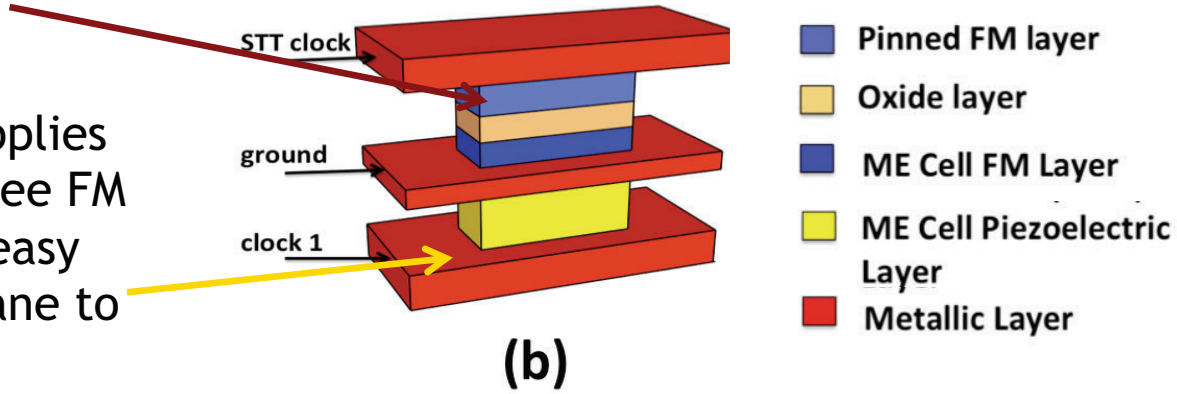




Need transducers to interface with CMOS

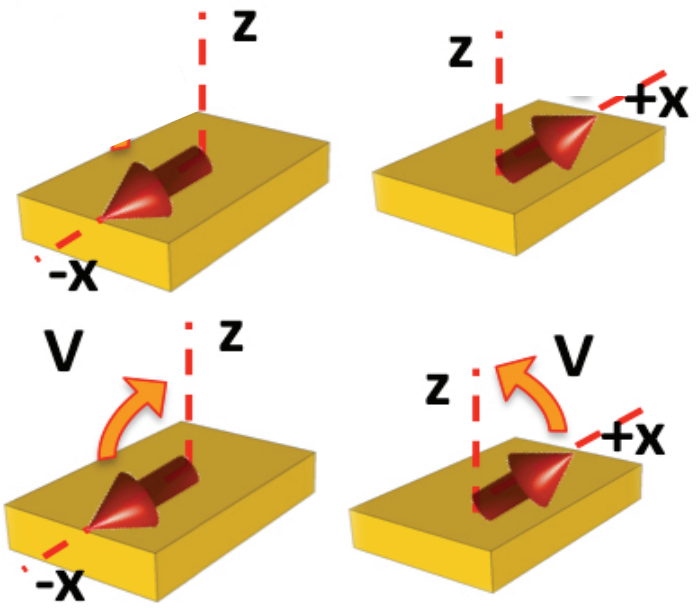
+ or – voltages applied to the pinned FM layer apply + or – spin currents to the free FM

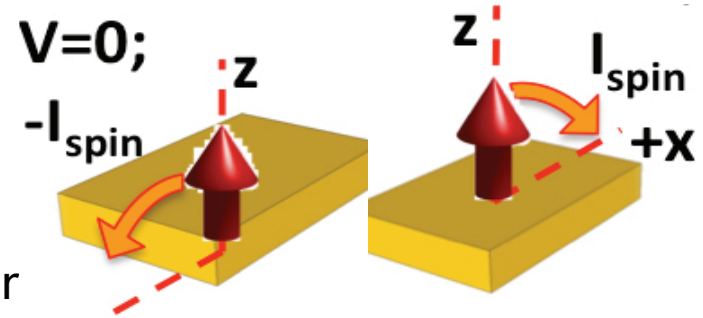
The Pz layer applies strain on the free FM to change the easy axis from in plane to out of plane.



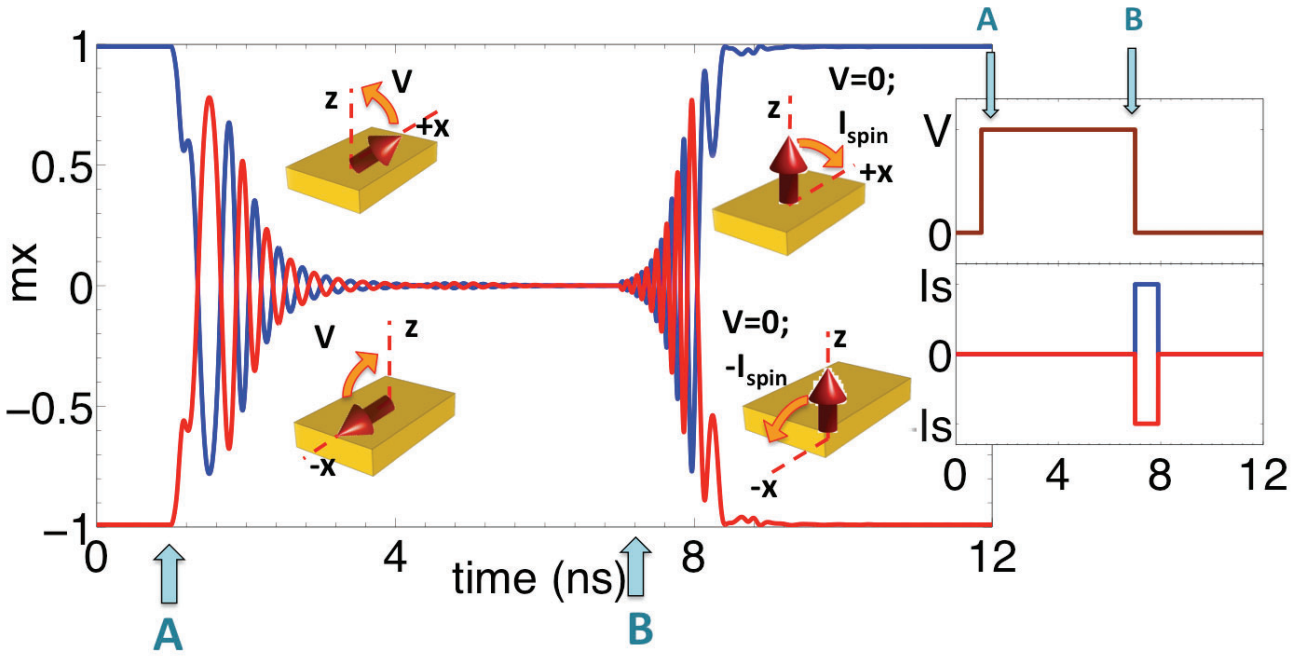
Charge to Spin (C-S) Transducer

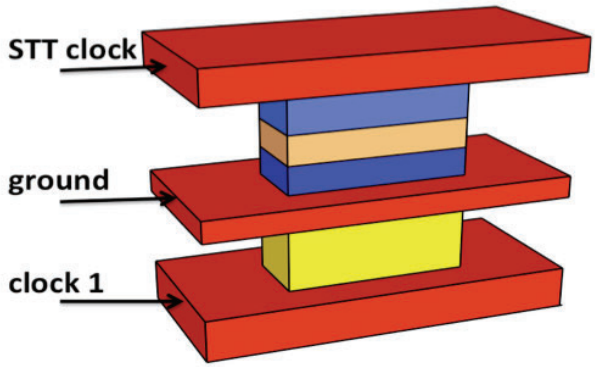
- If no voltage is applied to the Pz layer (clock= 0), the easy axis of the magnet is in plane.
- Data is saved as +x (1) or –x (0) magnetic orientations.
- Once the voltage is applied to Pz layer (clock=1), the strain applied on the magnet shifts the easy axis to out of plane.
- Depending on the original data (+x or –x) the generated spin wave has a phase of 0 or π.
- Once the clock goes back to zero, the easy axis goes back to in-plane but the magnet is momentarily in the meta stable.
- A spin current is used to push the magnet to either +x or –x directions and hence writing 1 or 0.



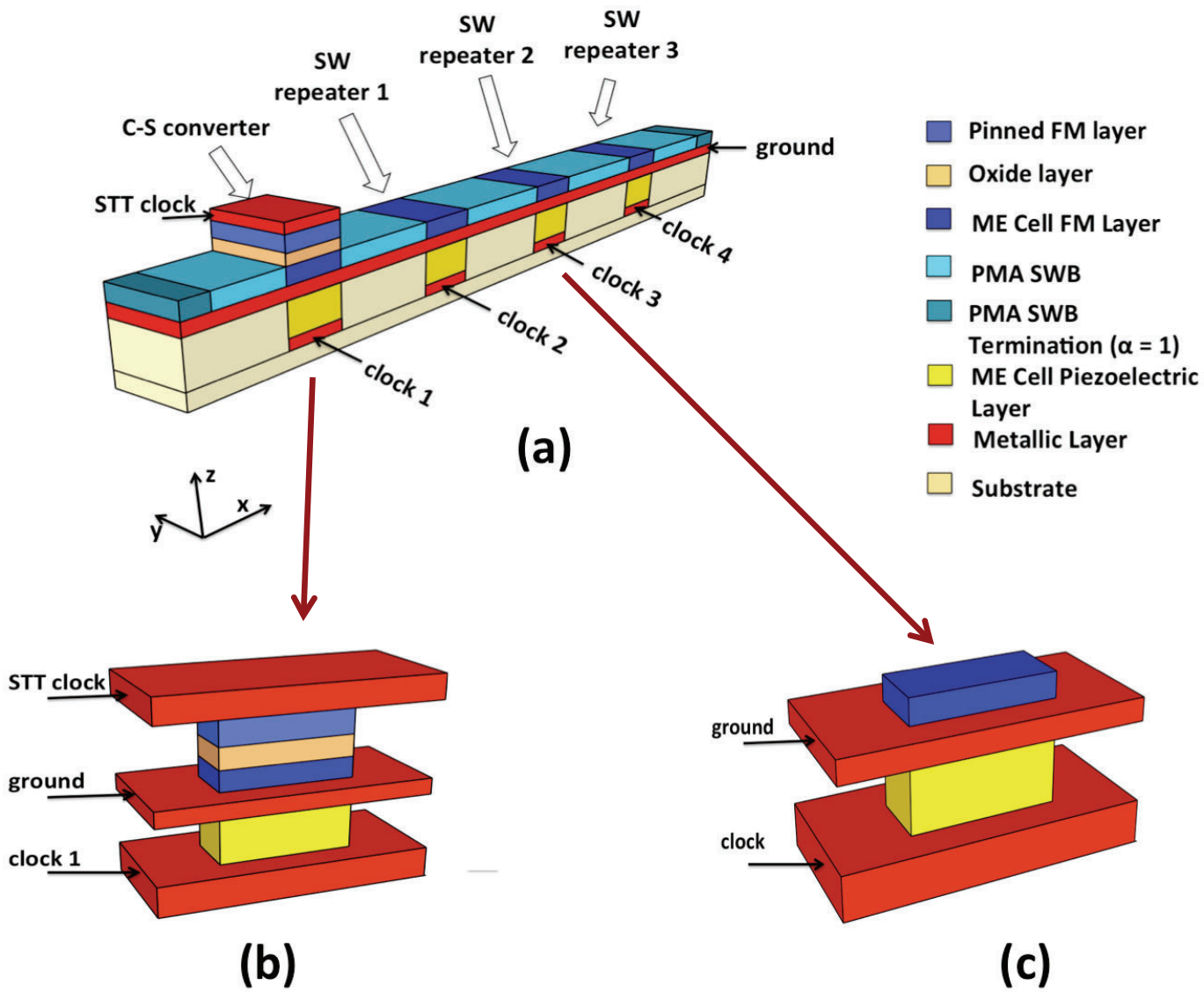


Charge to Spin (C-S) Converter





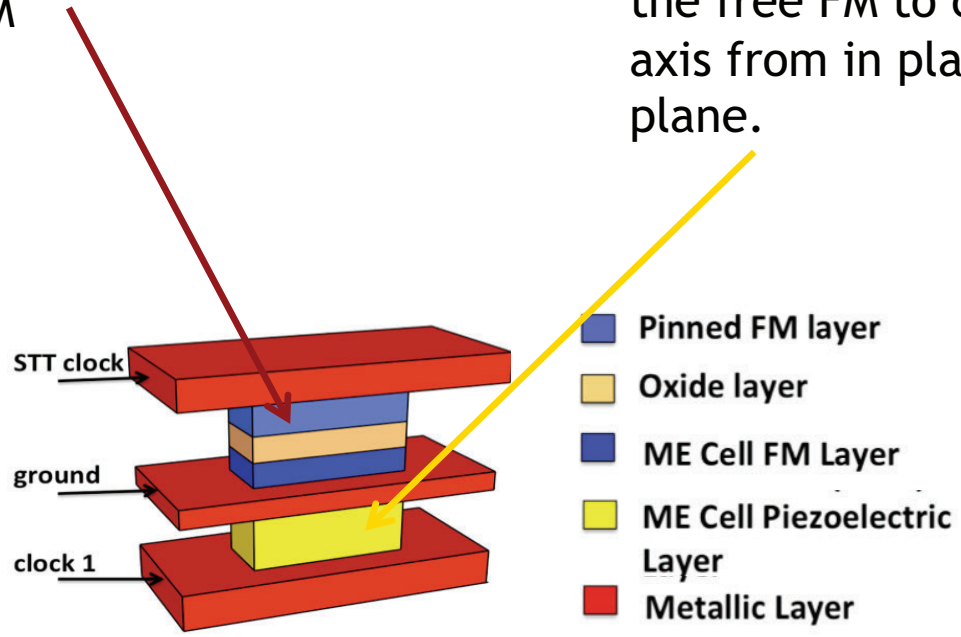
Clocked Cascaded Spin Wave Devices



Charge to Spin (C-S) Transducer

+ or – voltages applied to the pinned FM layer apply
+ or – spin currents to the free FM

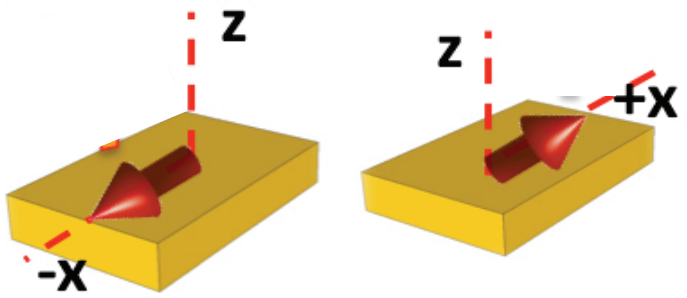
The Pz layer applies strain on the free FM to change the easy axis from in plane to out of plane.



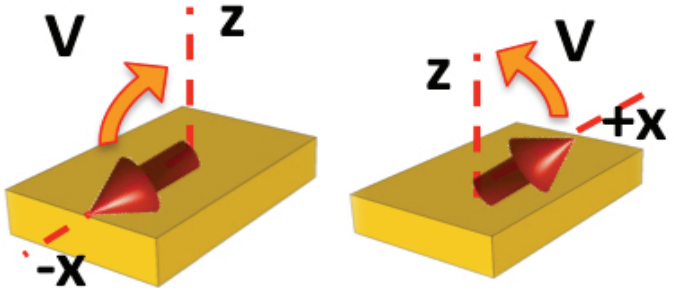
(b)

Repeater or Inverter

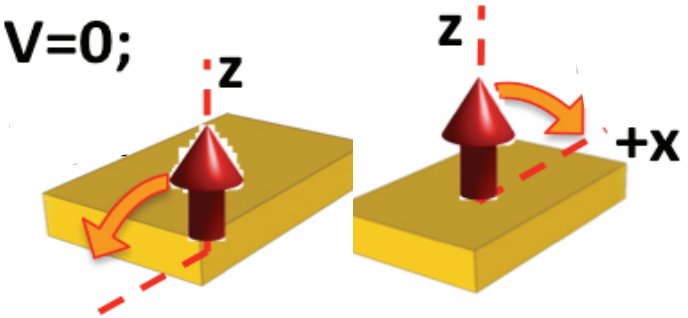
- If no voltage is applied to the Pz layer (clock= 0), the easy axis of the magnet is in plane.
- Data is saved as +x (1) or –x (0) magnetic orientations.



- Once the voltage is applied to Pz layer (clock,1), the strain applied on the magnet shifts the easy axis to the out of plane.

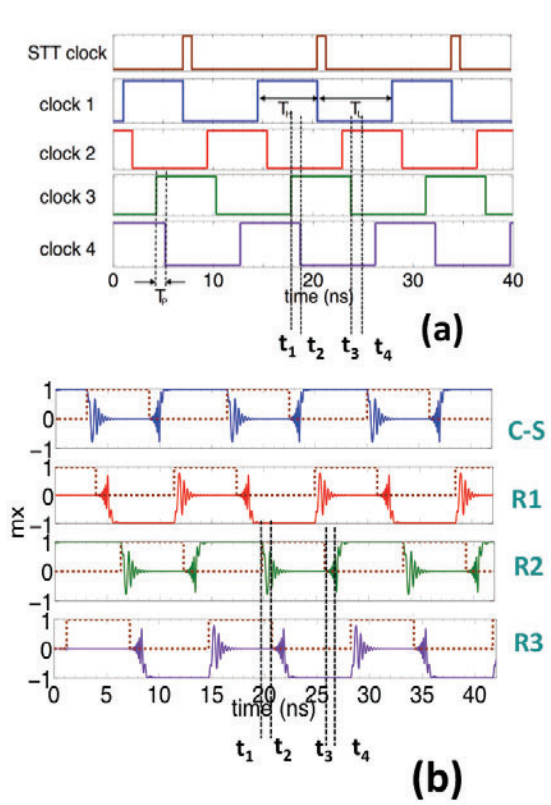


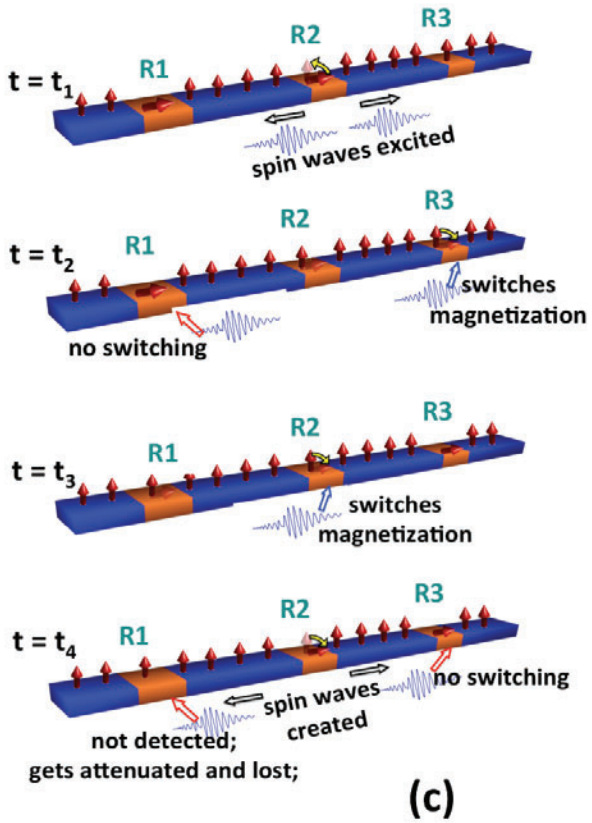
- Depending on the original data (+x or –x) the generated spin wave has a phase of 0 or π.
- Once the clock goes back to zero, the easy axis goes back to in-plane but the magnet is momentarily in the meta stable.
- The incoming spinwave pushes the magnet to either +x or –x directions and hence writing 1 or 0.



Clocking Scheme

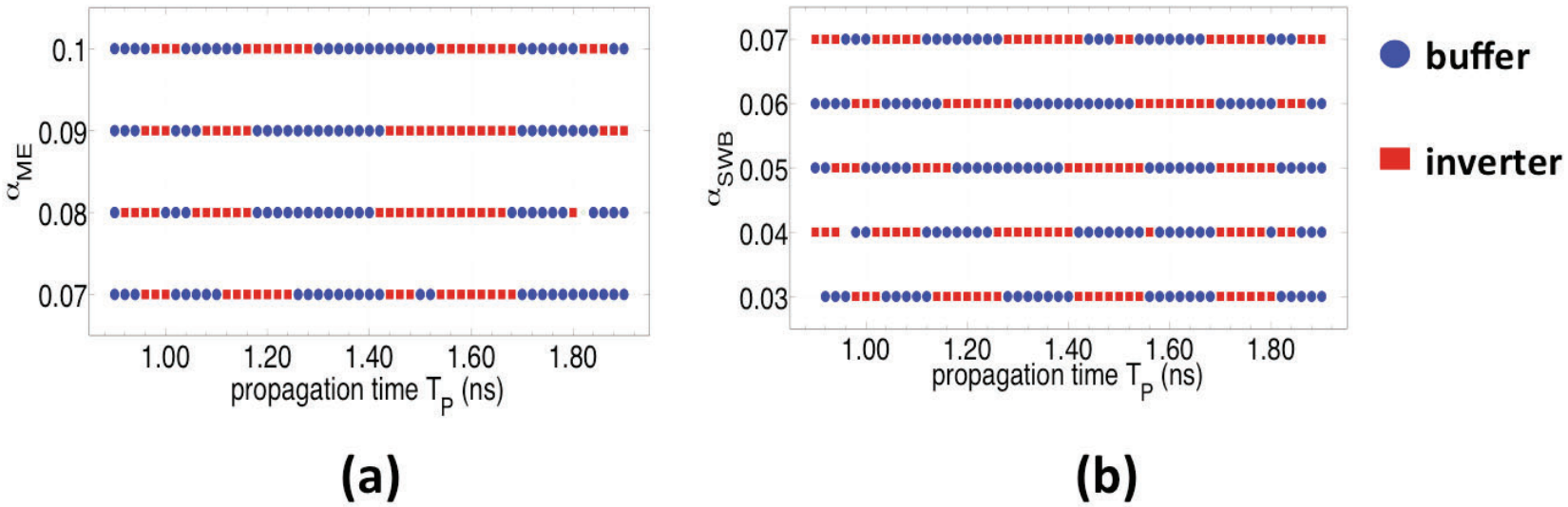
- Need for clocking
  - sequential transmission of information from one stage to the next
  - non-reciprocity
- Rising edge of the clock represents information transmission while the falling edge represents the detection and storage of signal.





Single stage device operation

- Sensitivity of the scheme as a function of the damping coefficient a_{ME} of the ME cell and the propagation time of the spin wave T_P



Conclusions

Beyond-CMOS devices may provide an alternative to geometrical scaling.

Fast and accurate models at various levels of abstraction are needed.

Cross-layer co-design and optimization are essential.

Material-level:

- Size effects can substantially shorten spin diffusion length in metals.
- Doping concentration improves resistivity but lowers spin diffusion length.
- Electric field increases spin relaxation length in Si to tens of micron.

Device-Level:

- Tunnel barriers can provide non-reciprocity and address impedance mismatch.
- Many reinventions and breakthroughs are still needed.

Conclusions

Circuit-Level:

- It is very difficult to beat CMOS in conventional circuits.
- SPICE models provide an insightful and flexible tool for analyzing spintronic devices and circuits.
- Novel circuit concepts that take advantage of the novel devices are essential.
- Spin wave devices and circuits enable wave computing and may provide a fundamentally new way of computing.

More Reading

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