

Ultra-low voltage, ultra-small mode volume silicon microring modulator

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Abstract: We show GHz modulation in a 2.5 μm radius silicon micro-ring, with only 150 mV peak-peak drive voltage and an electro-optic modal volume of only 2 μm^3 . The swing voltage and the micro-ring modulator are the smallest demonstrations so-far in silicon. The presented approach lays the ground work for a new class of high speed low voltage modulators enabling, seamless integration of nanophotonics with low voltage digital CMOS nano-electronics.

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1. Introduction: scaling the operation voltage of silicon modulators

Low voltage operation of nanophotonic modulators is an important condition for providing the future bandwidth needs via nanophotonic-electronic integration [1–7]. In particular, the operating voltage of silicon nanophotonic modulators must scale aggressively as rail voltages (V_{dd}) for digital nano-electronics scale to 600 mV in future CMOS platforms [8–11]. Hence, it is of great interest to pursue low voltage modulation methods that are silicon compatible. While several novel approaches using polymers [9–11], nano-wires [12], plasmonics [13,14], and nano-crystals [15] have been pursued, a high speed, low voltage modulator remains to be demonstrated on silicon. A low voltage swing modulation scheme can significantly reduce the total transmitter energy and footprint by reducing the drive electronic complexity compared to the existing schemes [16].

We show GHz modulation in a 2.5 μm radius silicon micro-ring, with only 150 mV peak-peak drive voltage and an electro-optic modal volume of only 2 μm^3 . We achieve the low drive voltage and ultra low switching energy operation by biasing the modulator near the optimum charge injection efficiency point of the electro-optic device. This feature is unique to carrier injection modulators enabling ultra low voltage operation in contrast with other techniques for electro-optic structures [17–24]. The swing voltage and the micro-ring modulator are the smallest demonstrations so far in silicon. The presented approach lays the ground work for a new class of high-speed low-voltage modulators enabling seamless integration of nanophotonics with low voltage CMOS nano-electronics.

2. Ultra low mode volume (2.5 μm radius) microring modulator

We use a micro-ring of radius 2.5 μm , close to the bending loss limited footprint of micro-rings [25] in order to minimize both the energy and drive current requirements of the device.

The micro-ring is formed with a waveguide of width 500 nm coupled to 350 nm wide silicon waveguides (Fig. 1a). The transmission spectrum for TE-polarized light is shown in Fig. 1b.

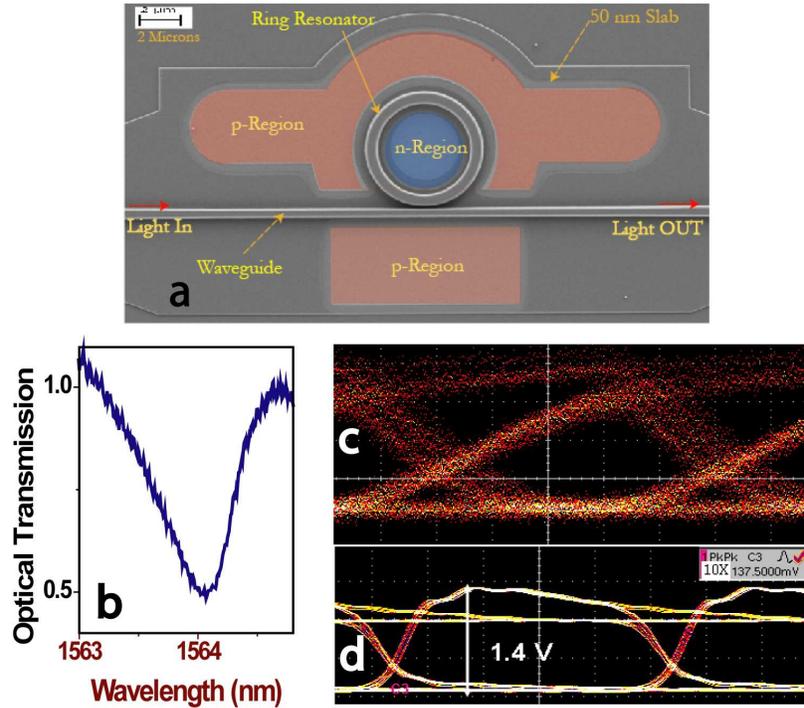


Fig. 1. a) SEM image of a silicon nanophotonic modulator created by embedding a 2.5 μm micro-ring in a PIN junction. b) Optical Transmission Spectrum of the Micro-ring normalised to non-resonant transmission c) Non-Return-to-Zero optical eye diagrams at 4 Gbps c) NRZ electrical driving signal at 1.4 V peak-peak biased at 0.5 V.

The micro-ring modulators are fabricated on silicon on insulator substrate. The top silicon layer (260 nm thick) is used for the passive waveguides and the electro-optic micro-ring modulator. The patterning steps are all performed with electron-beam lithography (JEOL 9300). We defined the silicon waveguides and the ring resonator and partially etched the silicon layer to a depth of 210 nm. Another lithography step was used to cover the modulator region and continue the silicon etch, leaving the 50 nm slab only around the modulator for the PIN diodes. After the etching, we deposited 20 nm SiO_2 for silicon passivation. Next, we performed the implantation steps for the p-region (outside the rings, BF_2 , dose $3 \times 10^{15}/\text{cm}^2$ at 45 keV) and n-region (inside the ring, Phosphorous, dose $2 \times 10^{15}/\text{cm}^2$ at 33 keV) respectively. A relatively low temperature anneal (650°C Rapid Thermal Anneal (RTA) for 120s) was subsequently used to activate the dopants. Nickel Silicide was then used for the electrical contacts to the modulator, with 15 nm evaporated nickel and 50 s rapid thermal anneal (RTA) at 550°C. We then deposited 1 μm SiO_2 top cladding, and patterned vias and contact pads connecting to the electrodes of the modulator. The sample was then diced and facet-polished to sub-wavelength roughness for testing. The device and Non-Return-to-Zero (NRZ) modulation waveforms are shown in Fig. 1, where we drove the modulator with NRZ data at 4 Gbit/s with a peak-peak voltage of 1.4 V biased at 0.5 V. We measured the optical transmission through the device using inverse tapered waveguide to fiber couplers at both ends of the chip [26]. A detailed description of the testing set up is provided in [27]. The insertion loss of the modulator comprising of the short section of the coupling waveguide and the ring is expected to be <0.1 dB. The fiber to fiber insertion losses are ~ 15 dB dominated by the fiber to waveguide coupling losses and the waveguide insertion loss.

3. Principle of operation for ultra low swing voltage in carrier injection modulators

We achieve very low swing voltage operation of PIN injection modulators by operating the modulator near the optimum charge injection point. Figure 2a shows the experimental and simulated IV characteristics of the micro-ring modulator. The mechanism for optical modulation is the free carrier dispersion due to the electron/hole concentration in the center of the waveguide [28], which we show in Fig. 2b as a function of voltage. The slope of this curve is the charge injection efficiency per volt (dQ/dv) shown in Fig. 2c. There is clearly an optimum charge injection region around a bias voltage of 1V. Here a change in voltage of only 100 mV produces a relatively large change in charge concentration of $2 \times 10^{17} \text{ cm}^{-3}$ inside the waveguide, corresponding to a refractive index change $\Delta n = 7.7 \times 10^{-4}$ [28].

The presence of an optimum charge injection region is due to the behavior of the carrier lifetime, which we illustrate here via an analytic model supported by electro-optic device simulations. The electro-optic simulations are in-turn validated against experimental steady state and transient performance of the modulator. The injected charge into the PIN diode can be extracted from the non-linear governing equation:

$$V(I) = V_t + IR + \frac{kT}{e\alpha} \log_e \left[\frac{I}{I_0} + 1 \right], \quad (1)$$

where I is the steady state current through the PIN diode, R is the total effective series resistance, k , Boltzmann constant, α the non-ideality coefficient of the diode, I_0 is the reverse saturation current. In Fig. 2, we show the analytical solution of the above equation along with the simulated and measured IV data. The fitting parameters are $I_0 = 90 \text{ nA}$, $V_t = 0.5 \text{ V}$, $\alpha = 0.62$, $R = 250 \text{ } \Omega$. The injected charge density can be obtained from the $V(I)$ characteristics following the non-linear governing equation for the steady state injected carrier density:

$$Q = I\tau_{recomb} = I \frac{\tau_0}{1 + \left(\frac{Q}{Q_0}\right)^n}, \quad (2)$$

where τ_0 is the carrier life time at low carrier densities, n is the power law dependence of the carrier lifetime with injected carrier density, Q_0 is a fitting parameter determined by the dependence of carrier lifetime on the minority carrier concentration in the PIN diode. We found n to be 1, indicating a recombination process that scales proportional to the carrier density [29]. The above equation can be obtained by the differential equation for injected charge in the diode at steady state by setting $dQ/dt = Q(t) - I/\tau_{recomb} = 0$. The results from Eqs. (1) and (2) can be combined to obtain the $Q(V)$ and, dQ/dv (shown in Fig. 2 c):

$$\frac{dQ}{dV} = \frac{dQ}{dI} \cdot \frac{dI}{dV} = G(V) \cdot \frac{\tau_0}{1 + \frac{Q}{Q_0}}, \quad (3)$$

where, $G(V)$ is the conductance of the diode obtained from (1). The calculated and simulated charge densities show excellent agreement to verify our assumptions. By biasing the modulator at high injection efficiency points (near the maxima of (3)), one can exploit the high charge injection (fC/mV) of the device to achieve a low voltage operation of the device.

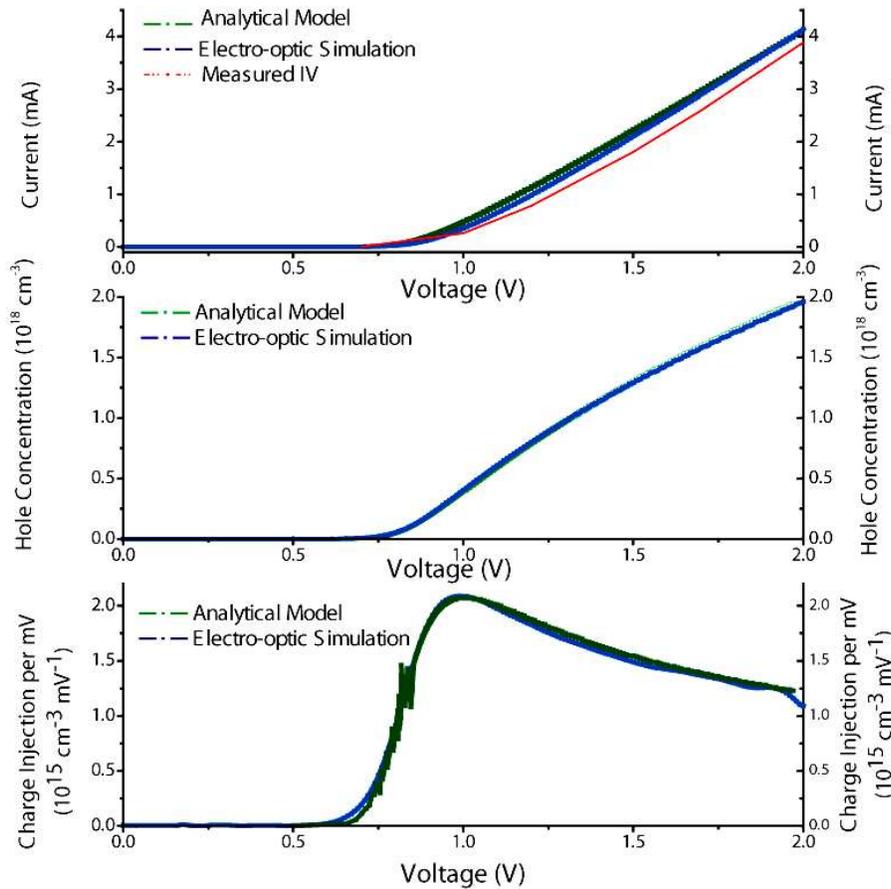


Fig. 2. a: Measured, simulated and analytical device I-V characteristics (red). b: Electron and hole concentrations in the waveguide (blue) c: Carrier injection per unit voltage (derivative of (b) with respect to voltage)

We simulated the transient carrier dynamics of the electro-optic modulator to verify the principle of operation. The electrical modeling was carried out in SILVACO ATLAS device simulation software and the optical modulation was calculated using an optical transmission matrix approach [30]. The software models the internal physics of the device by solving the Poisson equation and the charge continuity equation numerically. We included Shockley Read Hall (SRH), Auger, Direct recombination models. We assumed an interface trap density of $10^{10}/\text{cm}^2/\text{eV}$ and an interface recombination rate of 10^4 cm/s. The surface recombination rate of silicon is of the order of 10^4 cm/s for un-passivated surfaces and 100 cm/s for passivated surfaces. A detailed treatment of electro-optic modeling is presented in [28]. A good agreement between the measured and simulated waveforms can be observed in Fig. 3.

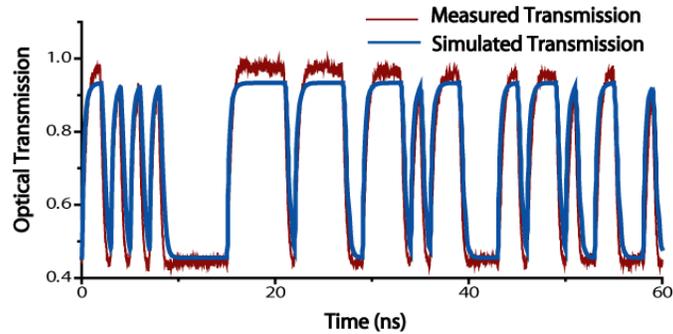


Fig. 3. Measured and simulated transient electro-optic device characteristics for the proposed operating conditions. The applied voltage is a square wave from 0.96 to 1.11 V.

4. Ultra low swing voltage modulation in carrier injection modulators

We demonstrate 1 Gbit/s modulation with a peak-peak drive voltage of only 150 mV. An eye diagram corresponding to the drive voltage is shown in Fig. 4 a. The output optical waveform generated by the silicon nanophotonic modulator at 1 Gbit/s NRZ is shown in Fig. 4 b. We drive the electro-optic modulator directly from the pattern generator using a 20 dB attenuator to obtain 150 mV voltage swing. A bias-tee is used to add a variable DC voltage to optimize the optical waveforms. The driving signal is terminated in a 50 ohm termination at the end of the high speed to probes to avoid reflections. A 150 mV voltage swing about a bias voltage level of 1.03 V was used to obtain clear waveforms. The optical eye diagram is shown in Fig. 4 b showing an open eye. We observe symmetric rise and fall times of ~ 1 ns corresponding to the recombination life time in silicon waveguides determined predominantly by the surface recombination processes.

We estimate the RF switching power consumed by the device to be 7.9 fJ/bit excluding the state hold power. The estimate of the switching power is arrived at as follows: The total charge injection times voltage swing provides the switching energy per injection. However, since 0-0, 0-1, 1-0, 1-1 transitions are all equally likely in a pseudo-random signal, the switching energy per bit is given by 1/4th of the switching energy per transition. The total charge injection for switching is estimated from the optical quality factor ($Q \sim 3000$), group index ($n_g = 4.262$) and modal volume of the cavity ($\Theta = 1.96 \mu\text{m}^3$) and free carrier dispersion in silicon [26]. The refractive index shift required for full optical switching across the ring is obtained from $\Delta n = n_g/Q_{\text{opt}} = 1.42 \times 10^{-3}$. This corresponds to an injected charge density of $\rho = 3.9 \times 10^{17} \text{ cm}^{-3}$. Hence the total charge injected is $\Phi = 251 \text{ fC}$ at each 0-1 transition. The energy per injection is therefore 37.7 fJ. However, since 0-0, 0-1, 1-0, 1-1 transitions are all equally likely in a pseudorandom signal [24], the switching energy per bit is given by 7.9 fJ/bit. However, we note that the total energy of the injection modulator is dominated by the DC power consumption given by $V_{\text{on}} I_{\text{on}} = e V_{\text{on}} \rho \Theta Q / \tau_{\text{recomb}} = 267 \mu\text{W}$

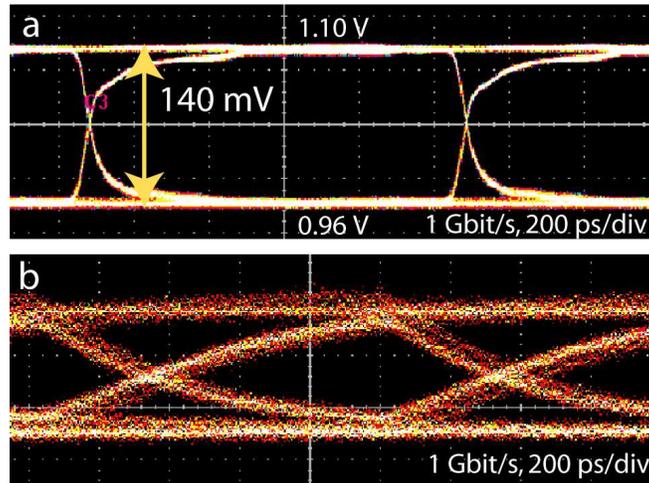


Fig. 4. Eye diagrams with 150 mV drive voltage at 1 Gbit/s for 2.5 μm micro-ring a) Input Voltage signal RF eye diagram with a swing voltage of 150 mV and a bias point at 0.96 V. modulator b) Output optical eye diagram measured from the silicon nanophotonic modulator

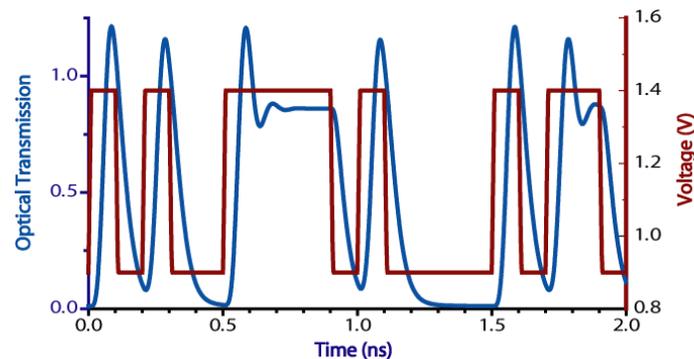


Fig. 5. Simulation of 10 Gbps electro-optic modulator with 500 mVpp drive voltage by decreasing the effective carrier lifetime to 100 ps.

The principle of operation presented here can also be extended to faster operating speeds. By controlling the carrier lifetime in the modulator [31], we expect that the speed of the modulators can be increased while still operating in the low drive voltage regime, with low loss waveguides [31]. In Fig. 5, we show simulation of 10 Gbps modulator operation with a 500 mV voltage swing by reducing the effective carrier lifetime. The SRH recombination rate is increased such that the effective carrier lifetime is 100 ps. The diode IV forward bias resistance is 110 ohm and the ring resonator loaded Q is 25,000, corresponding to a modest propagation loss of 17 dB/cm and photon lifetime of 21 ps.

5. Towards direct digital CMOS driven modulators

The proposed scheme can enable high-speed direct digital logic driven modulators that can be operated with a single stage (or tapered) inverters. We estimated the switching speeds of a scaled single stage digital logic driver. The maximum switching speed ($f_s = 1/t_{sw}$) for a single stage inverter (Fig. 6) [30] driven by minimum sized transistors is estimated as:

$$t_{sw} = 3 \frac{C_n V_n}{I_n} \cdot \frac{I_{modulator}}{I_n} + 1.5 \frac{C_n V_n}{I_n}, \quad (4)$$

where C_n, V_n, I_n are the capacitance, voltage and current through minimum sized transistor at a given technology node, $I_{\text{modulator}}$ is the peak current through the modulator. We plot the maximum switching speed of the direct logic drive as a function of the drive current for the modulator in Fig. 6. Gate lengths, voltages and delays are taken from ITRS 2009, Table PIDS2: High Performance Logic Technology Requirements [32,33]. One can clearly see that at 1 mA current levels for the present modulator, switching speeds approaching 10 GHz can be realised using direct CMOS digital logic drives. The estimated scaled NMOSFET channel width for a 1 mA drive current is expected to be $G_{\text{pmosfet}} = G_{\text{node}} \cdot I_{\text{modulator}} / I_{\text{d,sat mode}}$, assuming an $I_{\text{d,sat}}$ of $664 \mu\text{A}/\mu\text{m}$ at a 22 nm CMOS technology node [8]. This implies a drive transistor size of $1.5 \mu\text{m}$ which can scale down with current densities [8]. We note that the peak current in the device simulation shown in Fig. 5 is 3 mA, which corresponds to a scaled digital inverter cut-off bandwidth of 10 GHz in a 16 nm CMOS node. This reduction in footprint, driver energy, and complexity can enable seamless integration of nanophotonic with CMOS nano-electronics.

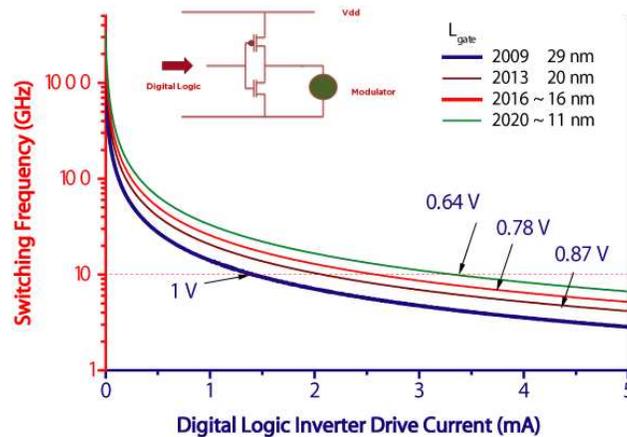


Fig. 6. Switching frequency of a single staged inverter driven directly with a digital logic level as a function of the drive current. The different colours indicate the switching frequency of the scaled digital layer inverter for various drive currents. A 10 GHz operation can be achieved for drive currents as large as 3 mA.

6. Conclusion

In conclusion, we demonstrate ultra-low drive voltage (150 mV) operation of carrier injection micro ring modulators in Gbit/s regime in an ultra low mode volume silicon micro-ring device. This low voltage driving scheme allows for direct digital logic driven modulators driven with micron sized transistors. To the best of our knowledge this is the smallest operating voltage (150 mV) for a GHz silicon modulator to date. The mode volume ($2 \mu\text{m}^3$, $(\sim 0.52 \lambda^3)$ & foot-print ($\sim 20 \mu\text{m}^2$) of the modulator is also the smallest to date for a micro-ring silicon modulator. The ability to scale the voltages of nanophotonic modulators down to few 100 mV may enable compatibility with future low voltage nano-electronic technologies beyond 22 nm CMOS, enabling close integration of nanophotonics with nano-electronics.

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