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Clocked Domain Wall Logic Using Magnetoelectric Effects

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ABSTRACT A new digital device scheme based on the magnetoelectric coupling and automotion of the magnetic domain wall is proposed. A single device is composed of a ferromagnetic wire and two ferroelectric capacitors served as the input and the output. It is shown that with the initialization in the magnetic states, a single device and the corresponding majority gate can realize the NOT, NAND, and NOR functions. Furthermore, the device has the cascadability, input–output isolation, gain, and nonreciprocity. The device concepts are justified by the numerical calculation, including the Landau–Lifshitz–Gilbert equation for the magnetization dynamics, the Landau–Khalatnikov equation for the electric polarization dynamics, and the electrostatic equations for the open-circuit output voltage and the charge sharing process between devices. The energy dissipation is also quantified and shown to be two to three orders of magnitude less than that in spin-torque-driven devices.

INDEX TERMS Domain walls (DWs), magnetoelectric (ME) effects, switched capacitor.

I. INTRODUCTION

OVER the past four decades, the exponentially increasing computing performance in a microchip has been a consequence of relentlessly scaling complementary metal–oxide–semiconductor (CMOS) integrated circuits based on Moore's law [1], which will sustain at least for another 15 years according to International Technology Roadmap for Semiconductors (ITRS) [2]. Meanwhile, active research in the field of the beyond CMOS technology is underway in pursuit of low-power logic and nonvolatile circuits [3], and one of the most explored beyond CMOS options is spintronics, where the electron spin is used as a computational variable [4].

Manipulating the electron spin using the current-induced spin torque has been extensively studied both theoretically and experimentally in the past decade [5]. Many spin-based devices or interconnects are proposed using spin current created by either spin injection directly from the ferromagnet (FM) [6]–[8] or the giant spin Hall effect [9]. However, based on the recent benchmarking results [10], [11], the energy associated with spin-torque-driven devices is much higher than that with CMOS transistors, and a potential solution to significantly reduce the energy in spintronics devices is controlling the magnetization using the electric field instead of the current. Therefore, it is of interest to explore a possible spintronic device structure to realize logic functions without passing any current through.

Recently, the magnetoelectric (ME) coupling has been under active research due to the possibility of the voltage-controlled magnetization switching [12], [13]. The ME coupling is the interaction between the electric polarization and magnetization, and has been observed in both a single material and a heterostructure [14]. However, a single material having the ME coupling is typically an antiferromagnet (e.g., Cr_2O_3), where the net magnetization is usually weak. Therefore, in this paper, we focus on the heterostructure showing the ME effect, which is defined as changing the magnetization by the electric polarization. The inverse ME (IME) effect is defined in a reverse order. Furthermore, in various material systems, the ME coupling can be induced by magnetostriction [15]–[19], charge transfer [20]–[28], or magnetic exchange bias [29], [30] at the interface. In particular, a successful ME magnetization reversal has been recently observed in a stack of multiferroic $BiFeO_3$ (BFO) and an FM [31]. In addition, a change in the electric polarization due to strain, induced by switching the

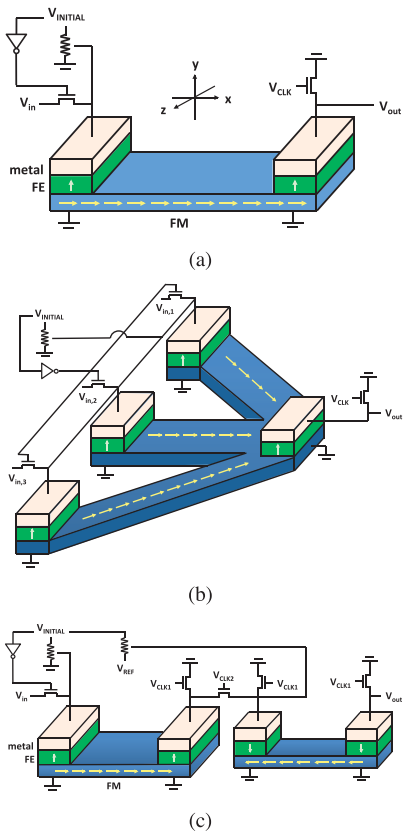

FIGURE 1. Proposed computational scheme using the ME effects. (a) Single device, (b) three-input majority gate, and (c) two devices in Cascade using a two-phase clocked circuit. Beige region: metal contact. Green region: FE. Blue region: FM. Green arrows: direction of the electric polarization of the FE. Yellow arrows: direction of magnetization of the FM. Under this scheme, logic 1 and 0 are represented by either voltage polarity or direction of the magnetization. A positive voltage and the magnetization pointing to the +x-direction stand for 1, and a negative voltage and the magnetization pointing to the −x-direction stand for −1. One of the possible setups for magnetization initialization is also shown.

magnetization through an external magnetic field, has been demonstrated in the layers of ferroelectric (FE) and ferromagnetic films [32]. As a result, based on these unique relations between the electric polarization and the magnetization, in this paper, a current-free spin-based logic device is proposed. A single device is composed of a ferromagnetic wire with two FE capacitors as the input and the output as shown in Fig. 1(a), where logic 1 and 0 are defined in both magnetization and voltage. The dominant mechanisms at the input and the output are ME and IME effects, respectively, which are used to create and detect the magnetic domain wall (DW). Due to no current flow in the FM wire, automotion of the DW [33] is in charge of propagating the magnetic signal from one end to another. Using the IME effect and a clocked switch, the voltage is established at the output when the magnetization of the wire is completely reversed. The output voltage can be used to drive the next stage by making the dimensions of connecting FE capacitors different, as shown in Fig. 1(c). To realize Boolean functions correctly, initialization of magnetic states is required before every computation, and thus, one of the possible circuits for initialization is also shown in Fig. 1.

The rest of this paper is organized as follows. In Section II, the operation principle of a single device is introduced, and how to Cascade devices is also mentioned. In addition, one of the possible circuits for magnetization initialization is presented. In Section III, the mathematical formalism, including the magnetization and electric polarization dynamics, the output open-circuit voltage, and charge sharing between two stages, is presented in detail. In Section IV, based on the developed theoretical models, a single stage is simulated to justify the device concept, and possible functions from a single device are discussed. In addition, a three-input majority gate using the proposed device and corresponding functions are predicted. Furthermore, the case of two connecting stages is simulated to show the device is cascadable, and the fan-out of the device is discussed. Finally, the energy dissipation associated with devices is estimated, and the conclusion is drawn in Section V.

II. DEVICE OPERATION

In this section, a single device operation and the principle of driving the next stage are described. A single device structure is shown in Fig. 1(a), where the ME and IME effects are used for the input and the output, respectively. For the input, an applied voltage pulse switches the electric polarization of the FE, and the electric polarization switches the magnetization through the ME coupling. The reversal of the magnetization underneath the input creates a DW, which can propagate from the input to the output automatically because of the demagnetization of the FM wire. Once the DW arrives the end of the FM wire, instead of reflection, the DW can disappear gradually by intentionally enhancing the damping mechanism at the end [34]. Thus, no signal is reflected back from the output, and the input–output isolation is achieved in the device.

To convert the output magnetic switching to the electric signal, instead of using the magnetic tunneling junction [35], which usually requires a complex sense amplifier associated with it [36], the IME combined with a clocked switch is used. The procedure of producing the output voltage is as follows. First, before the DW switches the magnetization underneath the output, the FE capacitor is connected to the ground by turning ON the switch. By doing this step, some charges are accumulated on the FE capacitor due to the nonzero electric polarization. Next, the switch is turned OFF to float the node, and thus, the amount of charge on the FE capacitor becomes fixed. When the magnetization at the output is reversed, the electric field due to the IME coupling is switched as well. However, the electric polarization is not fully switched accordingly, since the net electric field is compensated by another electric field in the opposite direction built up by the fixed charge on the capacitor; thus, the output

open-circuit voltage is generated. Based on the operating principle of a single device, a majority gate is proposed as shown in Fig. 1(b), where the computation is done within ferromagnetic wires [37]. Note that here no leakage through FE capacitors is assumed based on simulation parameters ($t_{FE} = 5$ nm). In reality, a significant leakage exists due to tunneling, bulk conduction, or conduction via defects if thickness of the FE is too thin (below 2 nm). As ME and IME coefficients are improved, the leakage can be largely reduced by a thicker FE layer (2 and 3). However, charge leakage would not ruin the operation of logic circuits, since the switching time is of the order of nanoseconds, which is too short for any appreciable charge to leak. Furthermore, in the steady state, it is not the charge but the magnetization that makes logic nonvolatile.

The cascadability of the devices can be realized by sharing the charge between two FE capacitors with another clocked switch as shown in Fig. 1(c), where CLK_1 is used to set up the charge and voltage at nodes, and CLK_2 is for passing the voltage from one node to another. Since there is no change in the magnetization at the input of the driven stage, the voltage remains zero before CLK_2 is ON. As a result, the input voltage of the driven device is always determined by the output voltage of the driving one, which provides the nonreciprocity of this computational scheme. Furthermore, the capacitance of the driven device is designed to be smaller than that of the driving one to make sure that the voltage after charge sharing is large enough for the DW creation. Fig. 2(a) and (b) shows the creation of the output open-circuit voltage and charge sharing between two devices.

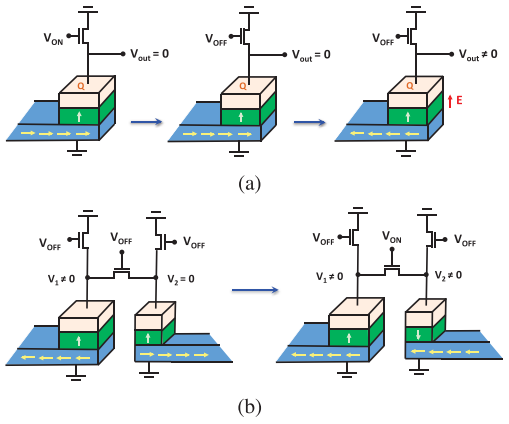

FIGURE 2. Schematics for (a) procedure of creating the output open-circuit voltage and (b) charge sharing process when connecting devices.

As will be shown in Section IV, initializing magnetic states in cascaded devices is required to produce correct logic functions. Thus, one of the possible circuits for initialization is shown in Fig. 1, where $V_{initial}$ is a clocked signal. When $V_{initial}$ is ON, the input signal is blocked by a clocked signal, which is complementary to $V_{initial}$, and an initialization signal is applied on devices through a voltage divider. The required antiparallel initial configuration shown in Figs. 7 and 8 is realized by different reference voltages on voltage dividers (e.g., 0 and V_{ref} in Fig. 1).

III. SIMULATION SCHEME

To model the proposed device, a numerical scheme describing the dynamics of the electric polarization and the magnetization with interface ME effects at both input and output is required. Therefore, in this paper, the Landau–Khalatnikov (LKh) equation is used to describe how the electric polarization evolves with time in the FE [38], and the Landau–Lifshitz–Gilbert (LLG) equation is used to describe the magnetization dynamics in the FM [39]. A single device is modeled by self-consistently solving the LKh and LLG equations together with the interface ME coupling. The induced open-circuit output voltage by the magnetization reversal is calculated using electrostatic equations. The numerical simulation scheme for a single device is shown in Fig. 3. Furthermore, when devices are cascaded, the charge sharing process is modeled by solving the current, electrostatic, LKh, and LLG equations together, and the corresponding numerical procedure is shown in Fig. 4. In this section, the mathematical details, including the ME coupling, electric polarization and magnetization dynamics, open-circuit output voltage, and charge sharing process, are given.

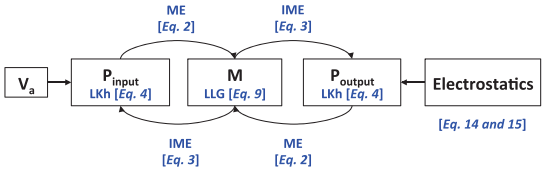

FIGURE 3. Simulation scheme for a single device. The LKh equations for the dynamics of the electric polarization at both input and output (P_{input} and P_{output}), the LLG equation for the dynamics of the magnetization (M), (2) and (3) for ME and IME effects, and (14) and (15) for the output open-circuit voltage are solved self-consistently to model the device.

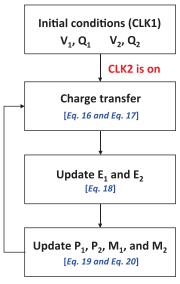

FIGURE 4. Numerical procedure to model a charge sharing process when devices are connected. The initial conditions are set by turning ON and OFF CLK1, and the charges are shared when CLK2 is ON. Subscripts 1 and 2 represent the output of the first stage and the input of the second stage, respectively.

A. INTERFACE MAGNETOELECTRIC COUPLING

As mentioned above, depending on different material systems, the ME coupling between the FE and the FM can be induced by strain, charge, or exchange bias at the interface.

Thus, instead of modeling the exact mechanism of each type of the ME (IME) effect near the interface, which is still an open problem in this field, here a general expression is attempted to describe the free energy, $F_{\mathrm{ME(IME)}}$, of all kinds of ME (IME) effects at the interface by introducing an experimental fitting parameter, $\alpha_{\mathrm{ME(IME)}}$, given as

$$F_{\mathrm{ME(IME)}} = -\alpha_{\mathrm{ME(IME)}} \frac{A t_{\mathrm{int}}}{\epsilon_0} P_i M_j \tag{1}$$

where A is the cross-sectional area of the FE/FM heterostructure, t_{int} is the thickness of the ME layer, ϵ_0 is the dielectric constant in vacuum, P_i is the electric polarization of the FE in the i-direction, and M_j is the magnetization of the FM in the j-direction. Note that theoretically, ME and IME effects should have the same α in the expression of the free energy [12]; however, experimental data show that α can be quite different between ME and IME effects [11], and the origin of this inconsistency is still under debate. Furthermore, without losing any essential physics, (1) assumes that the intermediate order involved in the ME (IME) coupling is well-coupled to the electric polarization or the magnetization. For instance, in the BFO/CoFe structure, the antiferromagnetic order of the multiferroic is assumed to be well-coupled to the electric polarization, and in the magnetostriction system, the strain is tightly bound to the magnetization. Typically, for different material systems, the range of α varies from $(100/c)$ to $(0.01/c)$ s/m, where c is the speed of light [11].

From the Landau theory, the effective magnetic field due to the interface ME coupling is given as

$$\vec{H_{\mathrm{ME}}} = \frac{-1}{\mu_0 A t_{\mathrm{FM}}} \frac{\partial F_{\mathrm{ME}}}{\partial \vec{M}} = \frac{t_{\mathrm{int}}}{t_{\mathrm{FM}}} \frac{\alpha_{\mathrm{ME}} P_i}{\mu_0 \epsilon_0} \hat{j} \tag{2}$$

where t_{FM} is the thickness of the FM and μ_0 is the free space permeability. Similarly, the effective electric field induced by the IME effect can be written as

$$\vec{E_{\mathrm{IME}}} = \frac{-1}{A t_{\mathrm{FE}}} \frac{\partial F_{\mathrm{IME}}}{\partial \vec{P}} = \frac{t_{\mathrm{int}}}{t_{\mathrm{FE}}} \frac{\alpha_{\mathrm{IME}} M_j}{\epsilon_0} \hat{i} \tag{3}$$

where t_{FE} is the thickness of the FE. As a consequence, for a given FE/FM heterojunction with ME and IME effects at the interface, the electric polarization of the FE inserts an effective magnetic field through the ME coupling on the FM, and the magnetization of the FM generates an effective electric field on the FE by the IME coupling.

B. DYNAMICS OF ELECTRIC POLARIZATION AND MAGNETIZATION

The time evolution of the electric polarization is governed by the LKh equation given as

$$\gamma_v \frac{\partial \vec{P}}{\partial t} = \vec{E_{\mathrm{eff}}} = -\frac{1}{V_{\mathrm{FE}}} \frac{\partial F_{\mathrm{FE}}}{\partial \vec{P}} \tag{4}$$

where $\vec{P}$ is the electric polarization, γ_v is the viscosity coefficient describing how fast the electric polarization can respond to the driving forces, $\vec{E_{\mathrm{eff}}}$ is the total effective electric field, and F_{FE} is the total free energy of the FE, including the Ginzburg–Landau–Devonshire term (F_{GLD}) with the expansion coefficients α_{FE1}, $\beta_{\mathrm{FE1,2}}$, and $\gamma_{\mathrm{FE1,2,3}}$ [40], the depolarization (F_{DP}) [41], and the applied electric field (F_{EXT}) given as follows:

$$F_{\mathrm{FE}} = F_{\mathrm{GLD}} + F_{\mathrm{DP}} + F_{\mathrm{EXT}} \tag{5}$$

$$\begin{aligned} F_{\mathrm{GLD}} = V_{\mathrm{FE}} \big[& \alpha_{\mathrm{FE1}} \left(P_x^2 + P_y^2 + P_z^2\right) \\ & + \beta_{\mathrm{FE1}} \left(P_x^4 + P_y^4 + P_z^4\right) \\ & + \beta_{\mathrm{FE2}} \left(P_x^2 P_y^2 + P_y^2 P_z^2 + P_x^2 P_z^2\right) \\ & + \gamma_{\mathrm{FE1}} \left(P_x^6 + P_y^6 + P_z^6\right) \\ & + \gamma_{\mathrm{FE2}} \big[P_x^4 \left(P_y^2 + P_z^2\right) + P_y^4 \left(P_x^2 + P_z^2\right) \\ & + P_z^4 \left(P_x^2 + P_y^2\right) \big] + \gamma_{\mathrm{FE3}} \left(P_x^2 P_y^2 P_z^2\right) \big] \end{aligned} \tag{6}$$

$$F_{\mathrm{DL}} = \frac{V_{\mathrm{FE}} \lambda_{\mathrm{NM}}}{t_{\mathrm{FM}}} \frac{P_y^2}{\epsilon_{\mathrm{DL}} \epsilon_0} \tag{7}$$

$$F_{\mathrm{EXT}} = -V_{\mathrm{FE}} (E_x P_x + E_y P_y + E_z P_z). \tag{8}$$

In (7), λ_{NM} is the metal screening length and ϵ_{DL} is the dead layer permittivity. E_x, E_y, and E_z in (8) are the applied electric fields in the x-, y-, and z-directions, respectively. For simplicity, the FE is assumed to be monodomainlike and is free from the effects of thermal noise; thus, the FE nearest-neighbors coupling [42], the dipole–dipole interaction, and the thermal fluctuations are ignored in the FE. The Euler scheme is used to integrate the LKh equation numerically. On the other hand, the LLG equation is used to describe the magnetization dynamics in the FM given as

$$\frac{\partial \vec{m}}{\partial t} = \alpha \left(\vec{m} \times \frac{\vec{m}}{\partial t} \right) - \gamma \mu_0 (\vec{m} \times \vec{H_{\mathrm{eff}}}) \tag{9}$$

where α is the Gilbert damping coefficient, $\vec{m}$ is the magnetic unit vector ($\vec{M} = M_s \vec{m}$), γ is the gyromagnetic ratio, and $\vec{H_{\mathrm{eff}}}$ is the effective magnetic field, including ME coupling ($\vec{H_{\mathrm{ME}}}$), material anisotropy ($\vec{H_{\mathrm{mat}}}$), shape anisotropy ($\vec{H_{\mathrm{sh}}}$), and exchange interaction ($\vec{H_{\mathrm{ex}}}$) shown as follows:

$$\vec{H_{\mathrm{eff}}} = \vec{H_{\mathrm{ME}}} + \vec{H_{\mathrm{mat}}} + \vec{H_{\mathrm{sh}}} + \vec{H_{\mathrm{ex}}}. \tag{10}$$

In (10), field components are given as

$$\vec{H_{\mathrm{mat}}} = \frac{2K_{\mathrm{mat},x}}{\mu_0 M_s} m_x \hat{x} + \frac{2K_{\mathrm{mat},y}}{\mu_0 M_s} m_y \hat{y} + \frac{2K_{\mathrm{mat},z}}{\mu_0 M_s} m_z \hat{z} \tag{11}$$

$$\begin{aligned} \vec{H_{\mathrm{sh},i}} = -M_s \Bigg(& \sum_j N_{xx,ij} m_{x,j} \hat{x} + \sum_j N_{yy,ij} m_{y,j} \hat{y} \\ & + \sum_j N_{zz,ij} m_{z,j} \hat{z} \Bigg) \end{aligned} \tag{12}$$

$$\vec{H_{\mathrm{ex}}} = \frac{2A_{\mathrm{ex}}}{\mu_0 M_s} \left(\frac{\partial^2 m_x}{\partial x^2} \hat{x} + \frac{\partial^2 m_y}{\partial y^2} \hat{y} + \frac{\partial^2 m_z}{\partial z^2} \hat{z} \right) \tag{13}$$

where $K_{\mathrm{mat},x}$, $K_{\mathrm{mat},y}$, and $K_{\mathrm{mat},z}$ are material anisotropy energy density in the x-, y-, and z-directions, respectively, M_s is the saturation magnetization, $N_{xx,ij}$, $N_{yy,ij}$, and $N_{zz,ij}$ are components of the demagnetization tensor [43] at the

*i*th domain due to the *j*th domain, and A_{ex} is the exchange constant. The LLG equation is numerically solved using the Runge–Kutta method. Note that for simplicity, thermal fluctuations are ignored in the effective fields.

C. OPEN-CIRCUIT VOLTAGE

Due to the fixed charge on the output FE capacitor, the open-circuit voltage is induced when the magnetization is reversed. This process can be described simply through electrostatic equations given as

$$\vec{E_o} = \frac{\vec{P_0} - \vec{P(t)}}{\epsilon_0} \tag{14}$$

$$\vec{V_o} = -(E_{o,x} l_{FE} \vec{x} + E_{o,y} t_{FE} \vec{y} + E_{o,z} w_{FE} \vec{z}) \tag{15}$$

where $\vec{E_o}$ is the electric field induced by the change in the electric polarization, which is a result from the magnetization reversal through the ME coupling, $\vec{P_0}$ and $\vec{P(t)}$ are the electric polarization before and after the DW reaches the end, respectively, $\vec{V_o}$ includes the induced open-circuit voltages in the *x*-, *y*-, and *z*-directions defined in Fig. 1(a), and l_{FE} and w_{FE} are the length and the width of the FE layer, respectively.

D. CHARGE SHARING

When the devices are connected together, the charges on the FE capacitors flow from one side to another depending on the voltage difference between connecting nodes. The charge dynamics between nodes can be described by iterating the current, electrostatic, LKh, and LLG equations given as

$$\vec{I} = \frac{\vec{V_i} - \vec{V_j}}{R_{ON}} = \frac{\Delta \vec{Q}}{\Delta t} \tag{16}$$

$$\vec{Q}(t + \Delta t) = \vec{Q}(t) \pm \Delta \vec{Q} \tag{17}$$

$$\vec{E} = \frac{-\left(\frac{Q_x}{A_x} + P_x\right)}{\epsilon_0} \hat{x} + \frac{-\left(\frac{Q_y}{A_y} + P_y\right)}{\epsilon_0} \hat{y} + \frac{-\left(\frac{Q_z}{A_z} + P_z\right)}{\epsilon_0} \hat{z} \tag{18}$$

$$\vec{P} = \mathrm{LKh}[\vec{E} + \vec{E_{IME}}(\vec{M})] \tag{19}$$

$$\vec{M} = \mathrm{LLG}[\vec{H_{ME}}(\vec{P})] \tag{20}$$

where $\vec{V_i}$ and $\vec{V_j}$ include voltages in the *x*-, *y*-, and *z*-directions at nodes *i* and *j*, respectively, $\vec{Q}$ includes Q_x, Q_y, and Q_z, which are charges accumulated at the FE surface in the *x*-, *y*-, and *z*-directions, respectively, A_x, A_y, and A_z are FE surface areas in the *x*-, *y*-, and *z*-directions, respectively, and R_{ON} is the ON-resistance of the switch. Equations (16)–(20) describe how the charge, electric field, electric polarization, and magnetization at either node *i* or *j* evolve with time.

IV. RESULTS AND DISCUSSION

In this section, a single device is simulated to show the ability to realize a NOT gate using the numerical scheme introduced above. Based on the operation of a single device, NAND and NOR gates are predicted using a three-input majority gate. The logical input and output states in these gates are encoded in magnetizations. Voltages are applied in order to switch magnetizations. Furthermore, the case of two devices in Cascade is also simulated to demonstrate the ability to propagate the signal from one stage to another through a two-phase clocking scheme. Finally, the energy dissipation of the device is quantified.

The simulation parameters are summarized in the Supplementary Materials, where $BaTiO_3$ is used for the expansion parameters of the FE, a typical in-plane magnet is applied for a fast DW velocity [44], and the viscosity coefficient is chosen to make the time for switching to the saturation polarization roughly equal to 30 ps [10]. Note that in this paper, there is no hysteresis loop in the FE, since a very thin film is used [45]. In the proposed device, it is not required to have an FE hysteresis loop to make the device work normally. For the input, the ME coefficient is chosen to be larger than the IME one, so that a smaller voltage can be used to overcome the electric field due to the magnetization. For the output, to reduce the magnetic field induced by the electric polarization so that the DW can reach the end of the FM wire, the IME coefficient is chosen to be larger than the ME one. For simplicity, the coupling between the electric polarization in the out-of-plane direction of the FE (*y*) and the magnetization in the easy axis (*x*) is assumed. The Cartesian coordinate used for simulations can be found in Fig. 1(a).

A. SINGLE DEVICE

For a single device shown in Fig. 1(a), when a positive voltage is applied to the input, a negative electric field is generated across the FE and switches the electric polarization from the positive to the negative direction. The switching in the electric polarization reverses the direction of the magnetic field induced by the ME effect. If the magnetic field is strong enough, the magnetization close to the input will be flipped and the DW is created. The DW can automatically move throughout the FM wire by changing its shape due to intrinsic shape anisotropy. Once the DW reaches the output, it disappears because of a strong damping mechanism at the end [34], and the magnetization of the wire is completely switched. Note that before the DW arrives the output, the clock has to be turned ON and then OFF to provide some fixed charge on the FE capacitor. For the output, the electric polarization is not completely switched when the magnetization is reversed, since the IME electric field is compensated by a fixed-charge-induced electric field, which creates an open-circuit output voltage. On the other hand, if a negative voltage is applied, there is no change in the magnetization, and the output voltage remains zero.

Figures 5 and 6, which show the device works as described above, are the time evolutions of voltage, average magnetization, and electric polarization for a positive voltage and a negative voltage, respectively, with a single device having the initial magnetization in the $+x$-direction. Note that from Fig. 5, a voltage gain is obtained, which is mainly determined

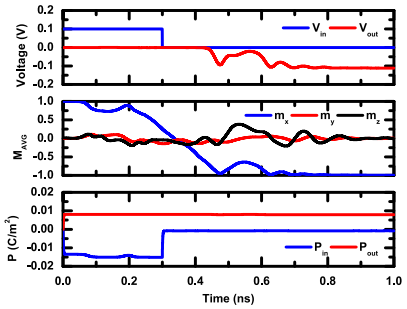

FIGURE 5. Voltage (V), average normalized magnetization (M_{AVG}), and electric polarization (P) as the functions of time for the case that the applied voltage is positive and the initial magnetization is in the $+x$-direction.

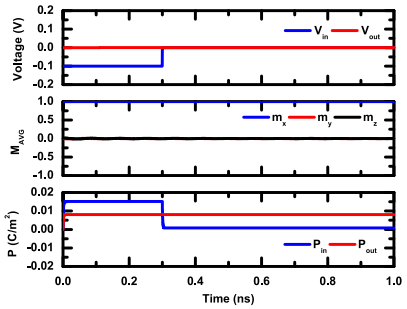

FIGURE 6. Voltage (V), average normalized magnetization (M_{AVG}), and electric polarization (P) as the functions of time for the case that the applied voltage is negative and the initial magnetization is in the $+x$-direction.

by the IME coefficient. In general, a larger IME coefficient results in a better magnetization-voltage conversion. The tradeoff between the energy and the switching delay is shown in the Supplementary Materials, and it is found that similar to the spin-torque-driven case [34], a greater voltage does not guarantee a shorter delay, since the DW velocity due to automotion is proportional to $\sin 2\phi$, where ϕ is the DW phase.

All the functions that a single device can provide are shown in Fig. 7(a), where the magnetization of the wire is totally determined by the input voltage regardless of the initial magnetization, and the output voltage is nonzero only when the switching in the magnetic state occurs. Note that positive and negative input voltages correspond to the final magnetization being $-x$ and $+x$, respectively. Therefore, the fact that the output voltage is opposite to the input voltage results in the opposite magnetizations in the consecutive stages and, thus, implements the NOT gate. Thus, to avoid logic computation errors induced by zero output voltages, the initial magnetizations of every stage are set to be antiparallel to each other as shown in Fig. 7(b), where for a NOT chain, positive and negative voltages correspond to completely opposite magnetic configurations. In other words, due to unique functions that the proposed device can provide, the error due to the zero output voltage can be removed by setting a correct magnetic state in the following stage initially. In addition, a correct output voltage can be deduced by

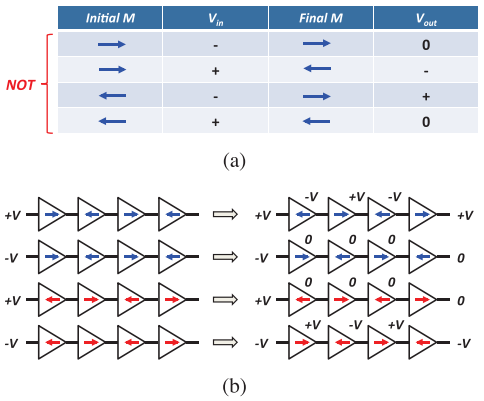

FIGURE 7. (a) Table summarizing all the functions provided by a single device shown in Fig. 1(a). (b) Schematic of a NOT chain, achieved by setting the initial magnetizations of every stage antiparallel to each other. Blue and red arrows: two opposite configurations of initial magnetization. For the same voltage, the final magnetic configuration remains the same no matter blue or red initial conditions are used.

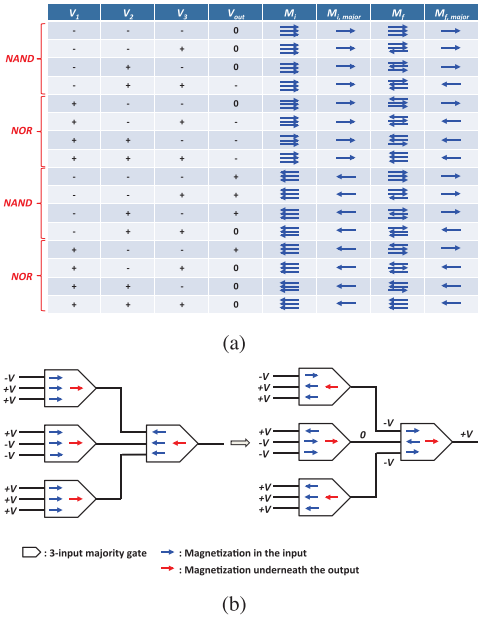

FIGURE 8. (a) Table summarizing all the functions provided by a three-input majority gate shown in Fig. 1(b). (b) Example of cascading three-input majority gates, where blue and red arrows represent the magnetizations in the inputs and underneath the output, respectively. Note that it is required to set the initial magnetic states of every stage antiparallel to each other for accurate computing results.

sensing the magnetization in the preceding stage if a zero output voltage is detected ($-x$: negative voltage and $+x$: positive voltage). Furthermore, NAND and NOR gates can be realized by implementing a majority gate based on the operation of a single device as shown in Fig. 1(b), where the computation is done in ferromagnetic wires and the majority of the magnetization determines the output voltage [37]. Fig. 8(a) shows all the functions in a three-input majority gate for the case that the magnetization of all three inputs is in the

either $+x$- or $-x$-direction. A NAND or a NOR gate can be determined by setting one of the inputs as a control terminal (e.g., $-$: NAND and $+$: NOR). Similarly, Fig. 8(b) shows an example that even though a zero output voltage may appear during the computation, one can still obtain correct magnetic states through the same magnetic initialization as mentioned above. Note that in Fig. 1, one of the possible circuits is shown to set up the initial magnetization of the FM wires, and the corresponding delay is the time needed for DW creation and transport to the end of the FM wire.

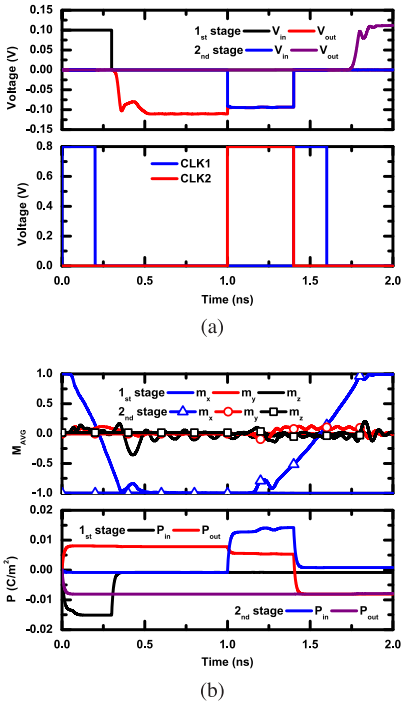

FIGURE 9. (a) Voltage, clock, (b) average normalized magnetization (M_{AVG}), and electric polarization (P) as the functions of time for the case that two devices are cascaded. The applied voltage is positive and the initial magnetizations of the first and second stages are in the $+x$- and $-x$-directions, respectively.

B. DEVICES IN CASCADE

Once the computation is done in a single stage, it is important to pass the signal to the next stage for implementing a more complicated function if a nonzero output voltage is generated. As a result, a two-phase clocking scheme is used for devices in Cascade as shown in Fig. 1(c), where CLK_1 and CLK_2 are used to set up and share the charge between nodes, respectively. Note that different from a single device mentioned previously, where the DW is created by the applied voltage, CLK_1 has to be turned ON and then OFF to set the initial charge on the FE capacitor after the DW is created and before the DW reaches the end. For CLK_2, the on-period needs to be long enough to make sure the DW can be generated in the FM wire. Fig. 9 shows the voltage, clock, average magnetization, and electric polarization as the functions of time for all the nodes in the case of two devices in Cascade. To drive the device in the second stage, the capacitance associated with the second stage is designed to be small enough compared with that with the first stage. The simulation parameters for two stages are also given in the Supplementary Materials. Again, since the magnetic state in the following stage is updated only when the output voltage is nonzero, it is important to initialize the magnetic states of every stage antiparallel to each other to ensure the computation is correct. Note that if there are more than one device in the next stage, to make sure the fan-out is large enough, the total input capacitance in the driven devices has to be small enough compared with the output capacitance of the driving one. For a logic circuit, a two-phase clocking scheme is especially useful for the situation that all the paths have the same logic depths and input data can be pipelined. For an unsteady data stream and a circuit with multiple logic depths, designing the clocks is nontrivial.

C. ENERGY DISSIPATION

Using the initialization setup shown in Fig. 1, the total energy associated with a single stage is composed of the energy for initializing magnetic states, the energy required to write the information through a voltage source, and the energy to turn ON CLK_1 for processing the charge at the output. Since a switch has to be turned ON for passing the input signal, a rough energy estimation for a single stage is given as

$$E_{\text{tot,single}} = C_{\text{FE}} V_{\text{FE}}^2 + C_g V_{\text{ON}}^2 \tag{21}$$

where C_{FE} is the FE capacitor calculated using the parallel-plate capacitor formula ($C_{\text{FE}} = (\epsilon_{\text{FE}}\epsilon_0 l_{\text{FE}} w_{\text{FE}}/t_{\text{FE}})$), V_{FE} is the writing voltage, C_g is the gate capacitor of a CMOS transistor, and V_{ON} is the voltage to turn a CMOS transistor ON. Similarly, the energy of a three-input majority gate is given as

$$E_{\text{tot,majority}} = 3C_{\text{FE}} V_{\text{FE}}^2 + 2C_g V_{\text{ON}}^2 \tag{22}$$

where two more inputs are needed to be initialized and written compared with (21). Furthermore, for the case of two stages in Cascade, the energy dissipation is given as below to account for additional clocks and initialized stage

$$E_{\text{tot,cascade}} = C_{\text{FE},1} V_{\text{FE}}^2 + \frac{1}{2} C_{\text{FE},2} V_{\text{FE}}^2 + \frac{5}{2} C_g V_{\text{ON}}^2. \tag{23}$$

Using the FE parameters in the Supplementary Materials ($C_{\text{FE}} = 0.12$ fF and $V_{\text{FE}} = 0.1$ V for a single stage and $C_{\text{FE},1} = 0.36$ fF, $C_{\text{FE},2} = 0.06$ fF, and $V_{\text{FE}} = 0.1$ V for two stages in Cascade) and the ITRS 2018 technology node for CMOS transistors ($C_g = 0.1$ fF and $V_{\text{ON}} = 0.72$ V), the energies are 53, 107, and 133 aJ for a single stage, a three-input majority gate, and two devices in Cascade, respectively, which are two to three orders of magnitude less than those in spin-torque-driven devices [10]. Note that rather than the ME switching, the energy dissipation in this scheme is dominated by the clocked switches. In addition, as mentioned previously, the FE capacitor in the driven stage has to be smaller compared with that in the driving one to

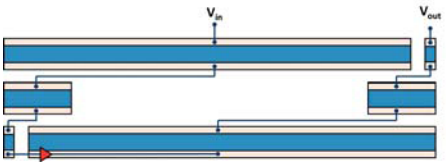

FIGURE 10. Top view of a possible layout for a NOT chain using the Cascade scheme shown in Fig. 1(c). A voltage amplifier (red triangle) working as a repeater is required whenever a smaller device is driving a larger one. The ratio of capacitances between stages is 6:1, which is used in Fig. 9 and can be further reduced by larger ME and IME coefficients at the input and the output, respectively. Note that the repeater buffer can be implemented with just an nMOSFET and a clock (i.e., nMOS dynamics clocked logic), since it is driving just a capacitive load.

pull the voltage high enough for the DW creation. As a result, if the device dimension cannot be shrunken anymore for a normal operation after a chain of multiple stages in Cascade, a voltage amplifier is required to work as a repeater for driving a larger device as shown in Fig. 10, where a possible layout for a NOT chain is presented. However, the stage ratio can be further reduced using heterojunctions with high ME and IME coefficients at the input and the output. For instance, if the ME coefficient at the input is increased, a small electric field will be enough to generate a magnetic field for DW creation. Hence, the required voltage for driving the next stage can be lower, and thus, the stage ratio is reduced.

V. CONCLUSION

In this paper, a new digital device scheme is proposed using the ME and IME couplings combined with automotion of the DW. By using the numerical simulations, the device is shown to be cascadable and to have the input/output isolation, nonreciprocity, and gain. In addition, the NOT, NAND, and NOR gates can be implemented by a single device and the corresponding majority gate with initializing magnetic states. Finally, it is shown that the proposed device based on the ME coupling dissipates much less energy compared with that using spin-transfer torques.

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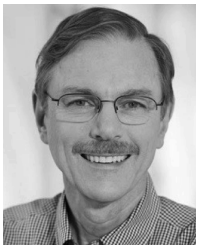

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